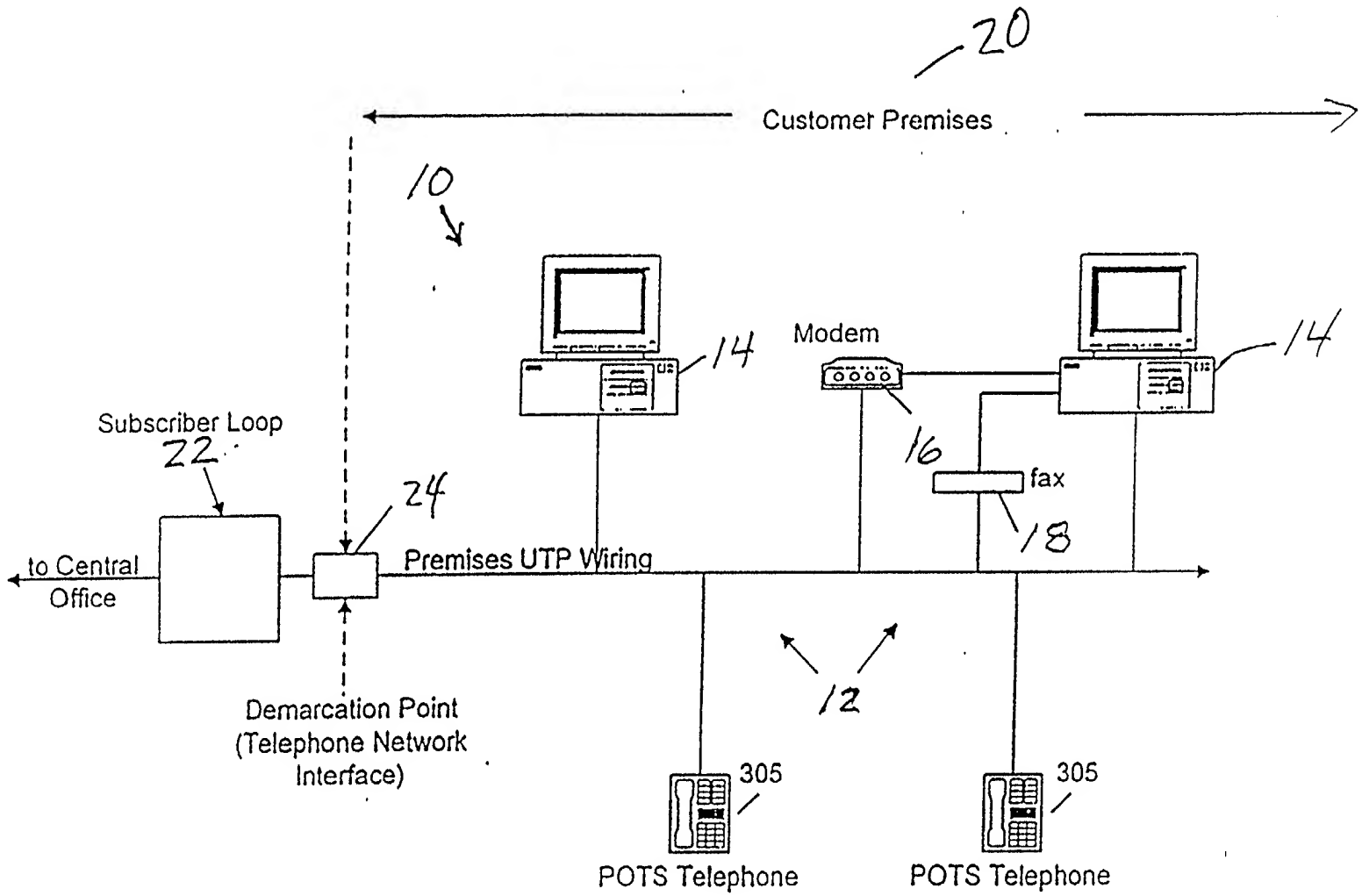

20
Customer Premises
10
14
Modem
14
16
fax
18
Subscriber Loop
22
24
to Central
Office
Premises UTP Wiring
Demarcation Point
(Telephone Network
Interface)
12
305
305
POTS Telephone
POTS Telephone

FIG. 1a

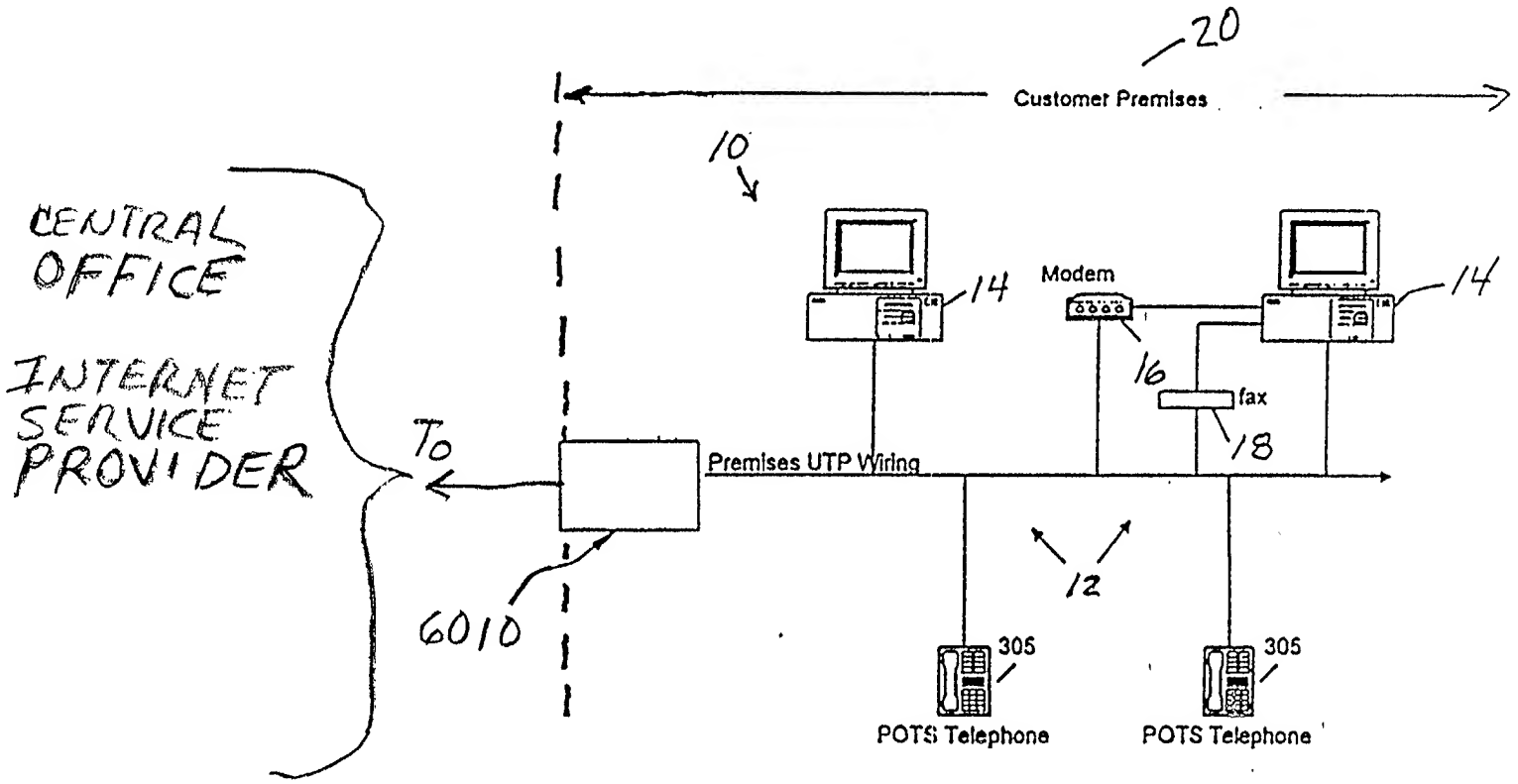
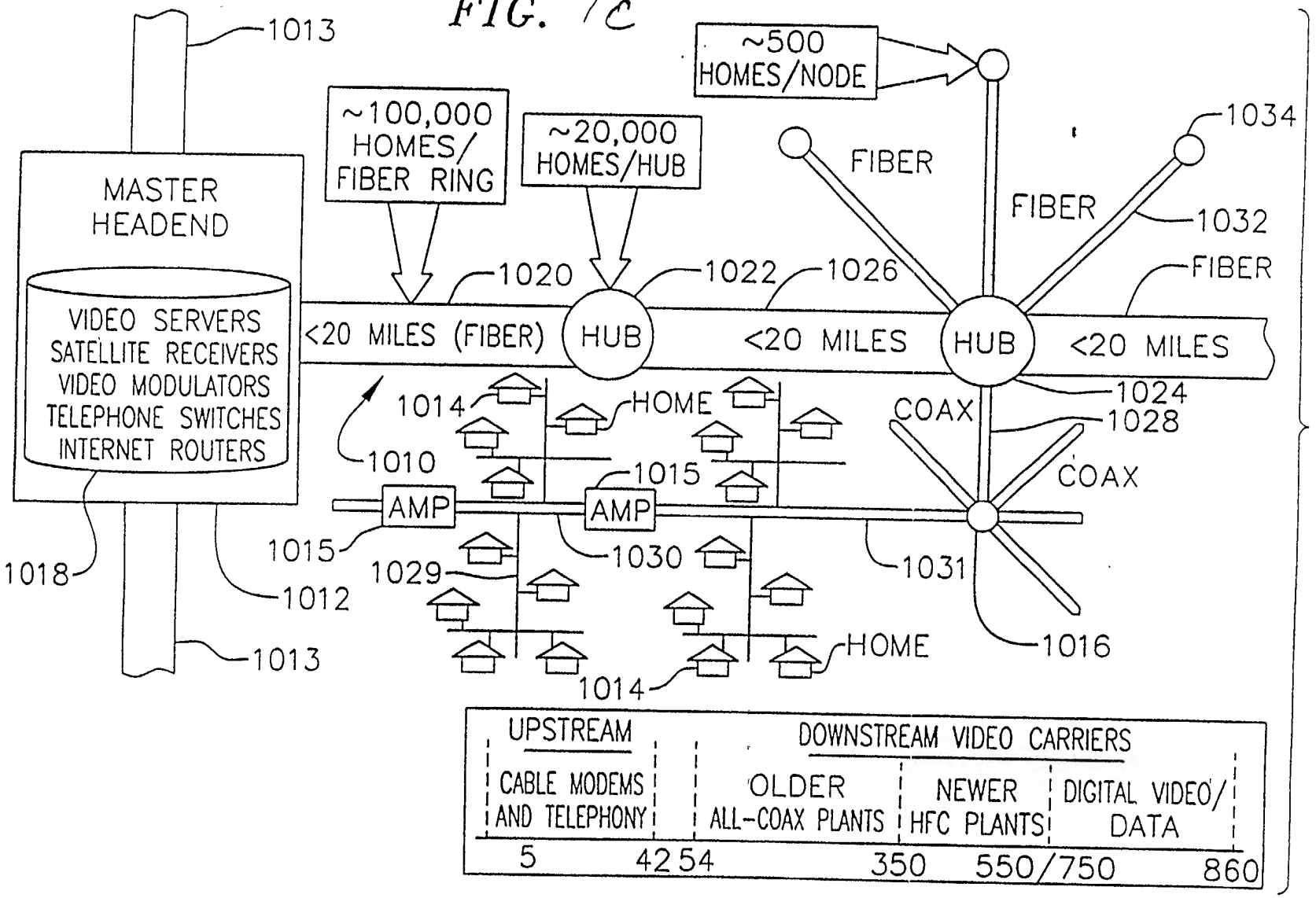

20
Customer Premises
10
CENTRAL OFFICE
INTERNET SERVICE PROVIDER
To
14
Modem
14
16
fax
18
Premises UTP Wiring
12
6010
305
POTS Telephone
305
POTS Telephone

FIG. 1b

FIG. 1C


1013
~500 HOMES/NODE
~100,000 HOMES/ FIBER RING
~20,000 HOMES/HUB
1034
FIBER
FIBER
1032
MASTER HEADEND
VIDEO SERVERS
SATELLITE RECEIVERS
VIDEO MODULATORS
TELEPHONE SWITCHES
INTERNET ROUTERS
1020
1022
1026
FIBER
<20 MILES (FIBER)
HUB
<20 MILES
HUB
<20 MILES
1024
1014
HOME
COAX
1028
1010
1015
COAX
AMP
AMP
1015
1030
1031
1018
1029
1012
1013
HOME
1016
1014
UPSTREAM
DOWNSTREAM VIDEO CARRIERS
CABLE MODEMS AND TELEPHONY
OLDER ALL-COAX PLANTS
NEWER HFC PLANTS
DIGITAL VIDEO/ DATA
5
42 54
350
550/750
860

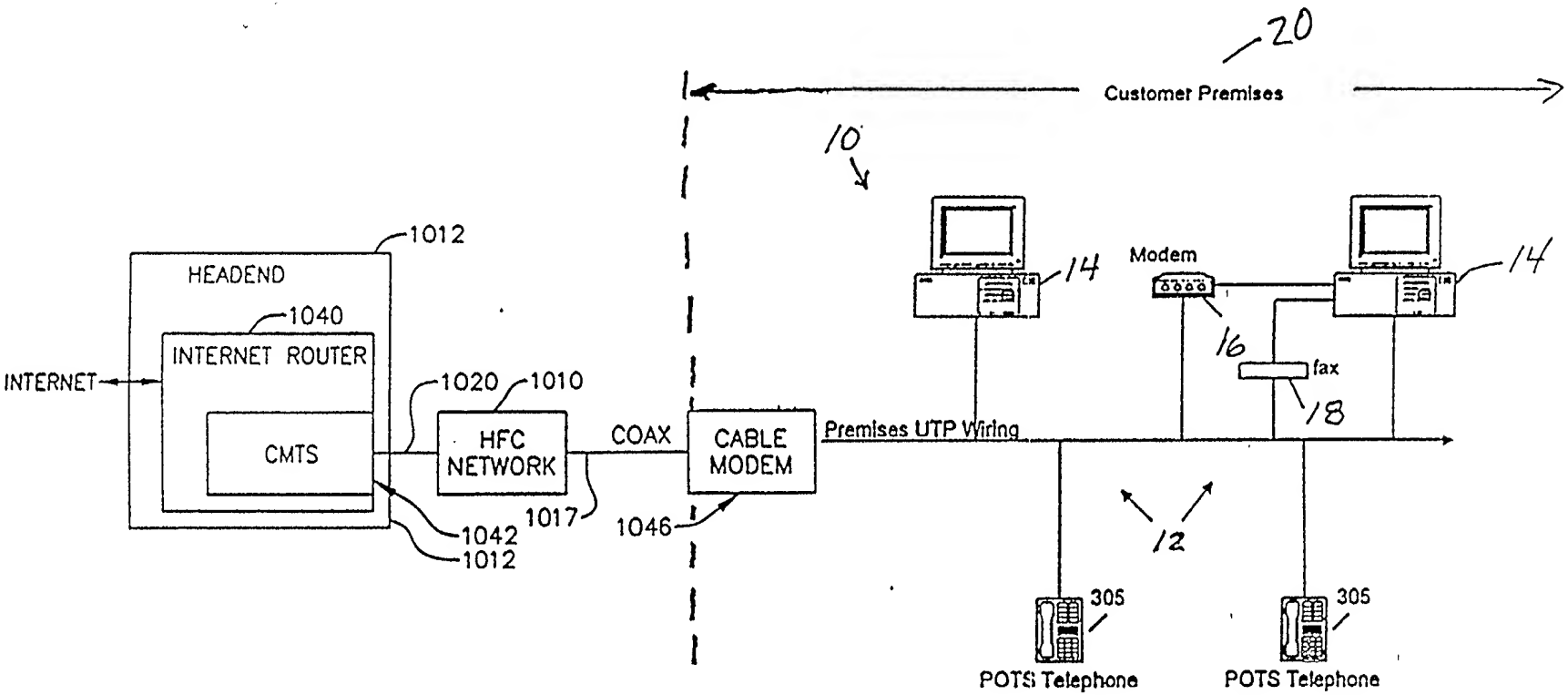

20
Customer Premises
10
1012
HEADEND
1040
INTERNET ROUTER
INTERNET
CMTS
1020
1010
HFC NETWORK
COAX
CABLE MODEM
1042
1012
1017
1046
Premises UTP Wiring
14
Modem
16
fax
18
14
12
305
POTS Telephone
305
POTS Telephone

Fig 1d

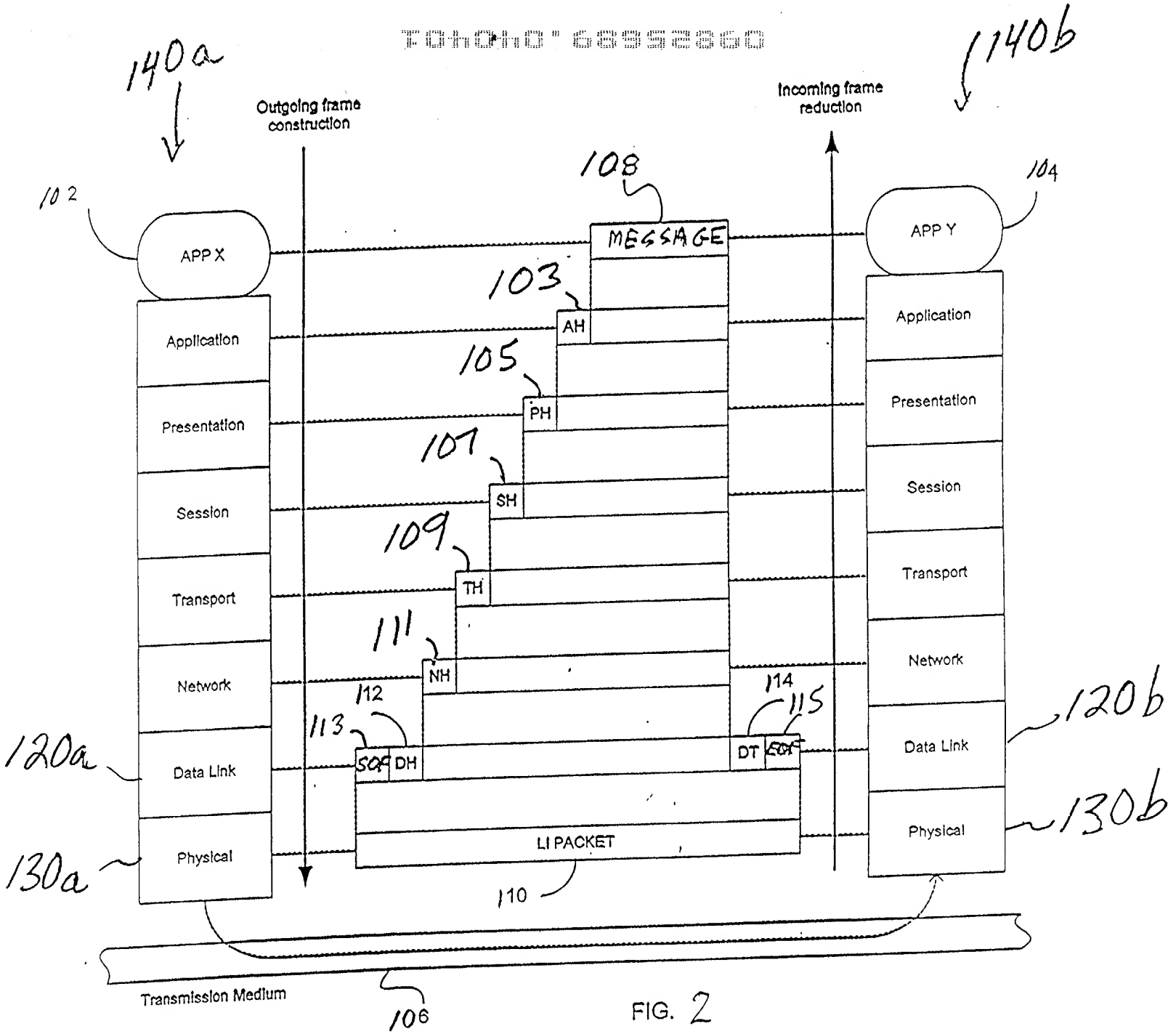

140a
140b
Outgoing frame construction
Incoming frame reduction
102
104
108
APP X
APP Y
MESSAGE
103
AH
105
PH
107
SH
109
TH
111
NH
112
113
114
115
SQF
DH
DT
EQF
LI PACKET
110
Application
Presentation
Session
Transport
Network
Data Link
Physical
120a
120b
130a
130b
Transmission Medium
106

FIG. 2

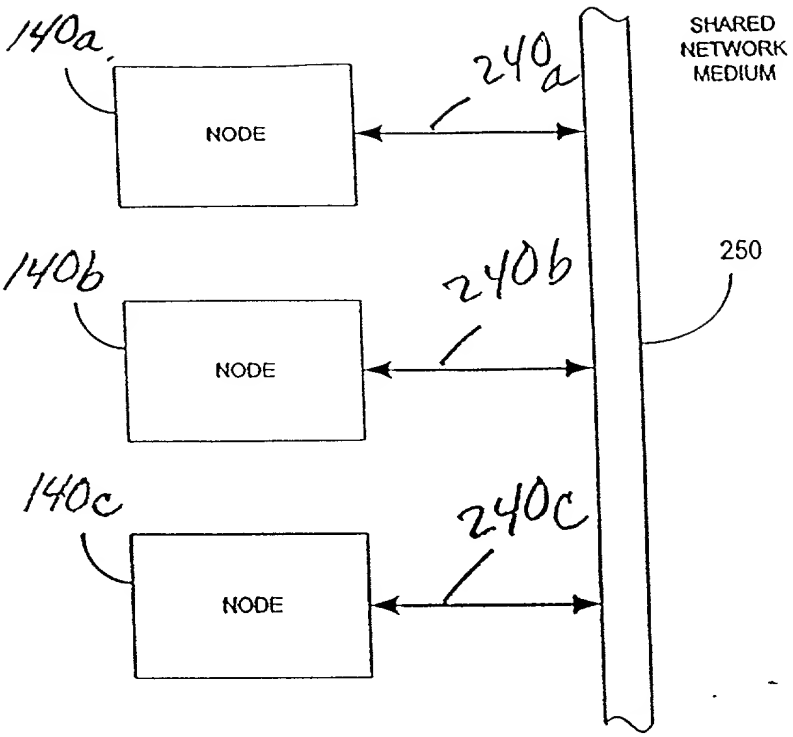

140a
NODE
240a
SHARED
NETWORK
MEDIUM
140b
NODE
240b
250
140c
NODE
240c

FIG. 3a

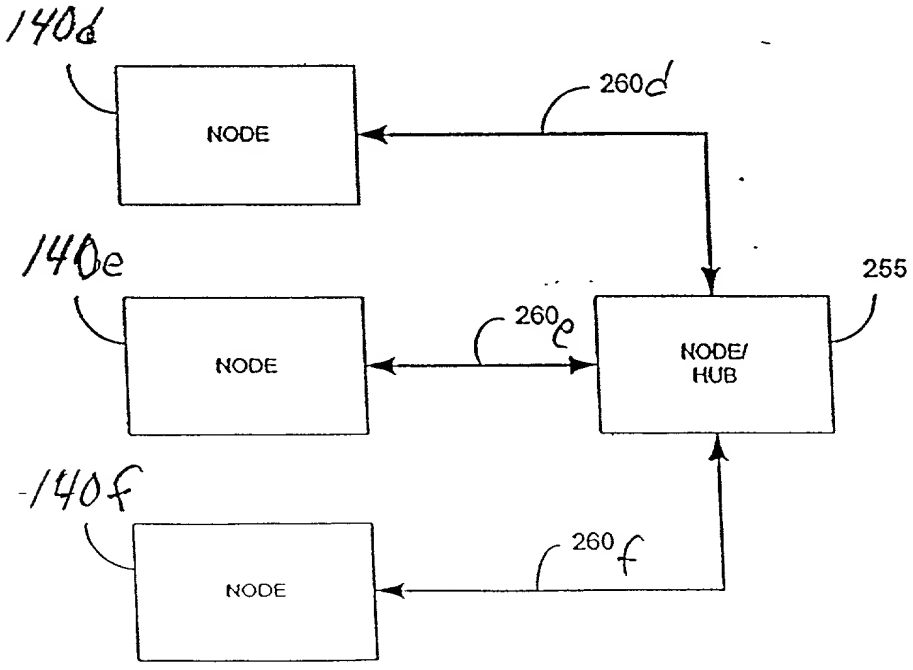

140d
NODE
260d
140e
NODE
260e
NODE/
HUB
255
140f
NODE
260f

FIG. 3b

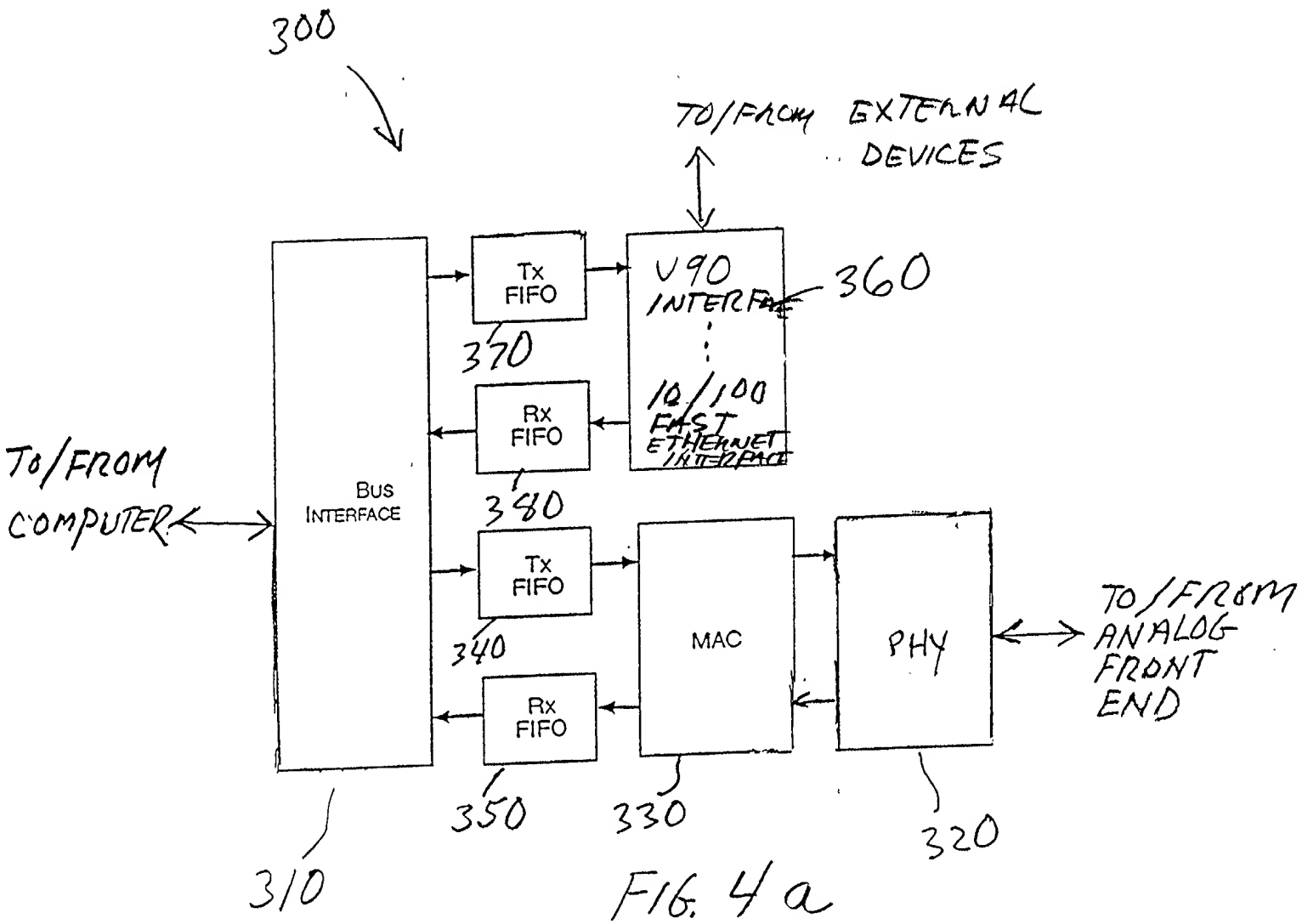

300
TO/FROM EXTERNAL DEVICES
V90 INTERFACE
360
10/100 FAST ETHERNET INTERFACE
Tx FIFO
370
Rx FIFO
380
TO/FROM COMPUTER
BUS INTERFACE
Tx FIFO
340
Rx FIFO
350
MAC
330
PHY
320
TO/FROM ANALOG FRONT END
310

FIG. 4a

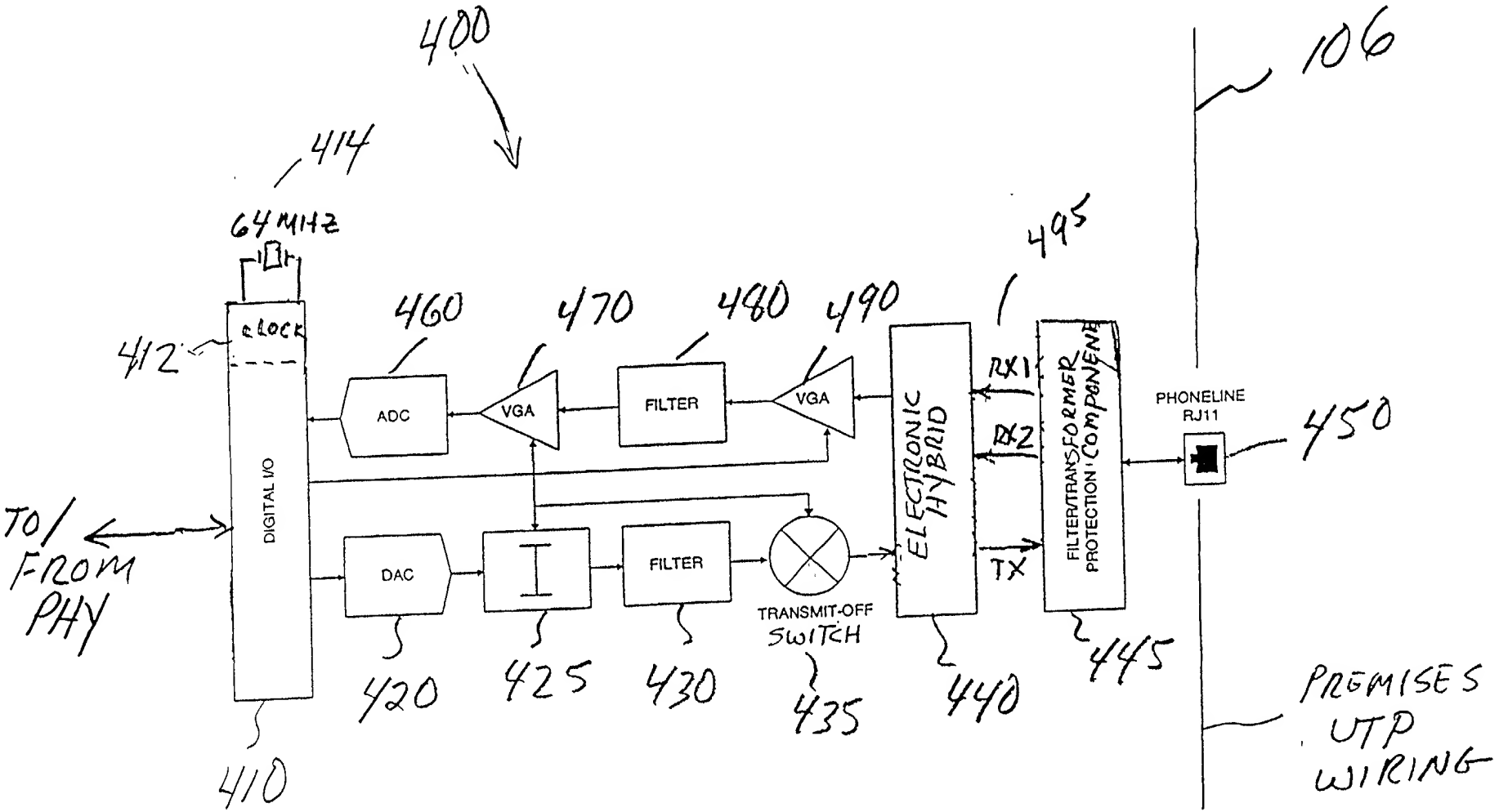

400
414
64 MHz
CLOCK
412
DIGITAL I/O
410
TO/FROM PHY
460
ADC
470
VGA
480
FILTER
490
VGA
DAC
420
425
430
FILTER
TRANSMIT-OFF SWITCH
435
ELECTRONIC HYBRID
440
495
RX1
RX2
TX
FILTER/TRANSFORMER PROTECTION COMPONENT
445
PHONELINE RJ11
450
106
PREMISES UTP WIRING

FIG 4b

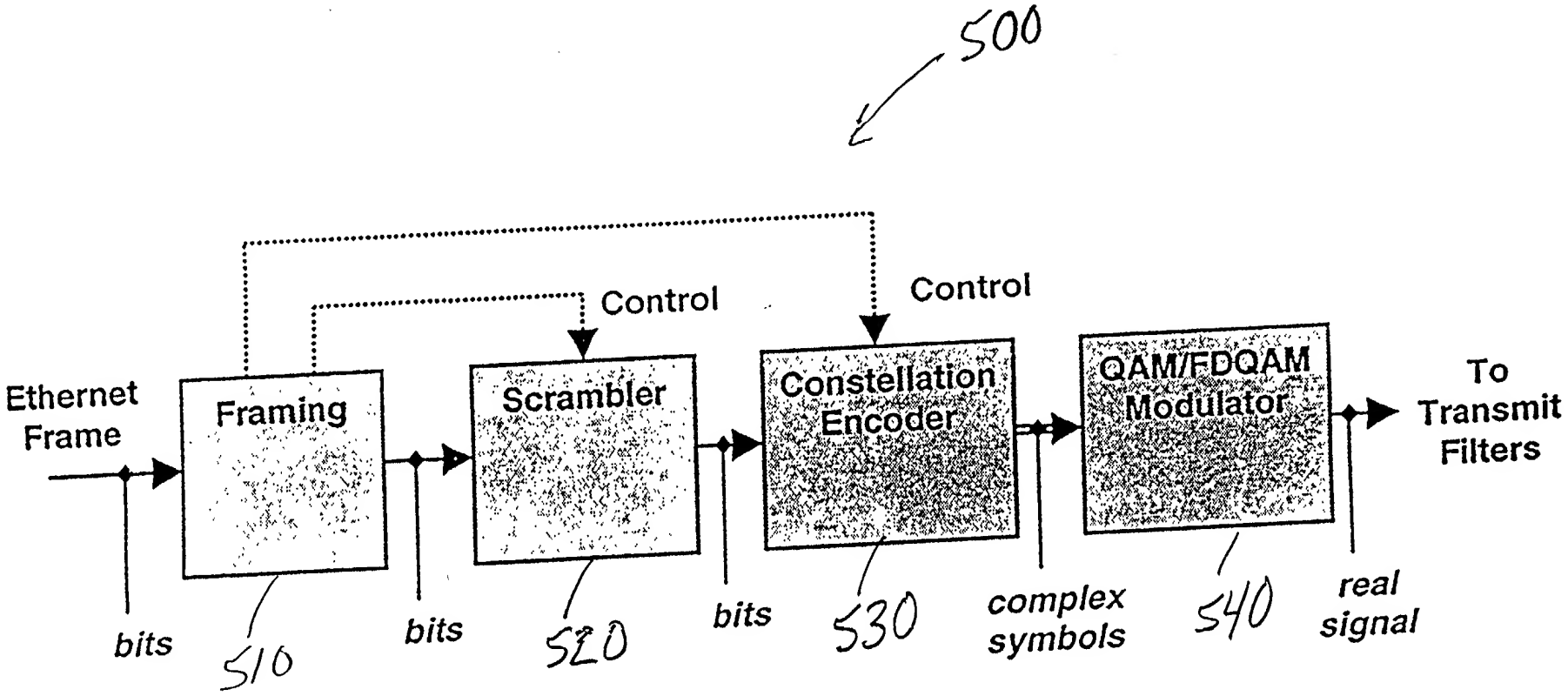

500
Control
Control
Ethernet Frame
Framing
Scrambler
Constellation Encoder
QAM/FDQAM Modulator
To Transmit Filters
bits
bits
bits
complex symbols
real signal
510
520
530
540

FIG 5

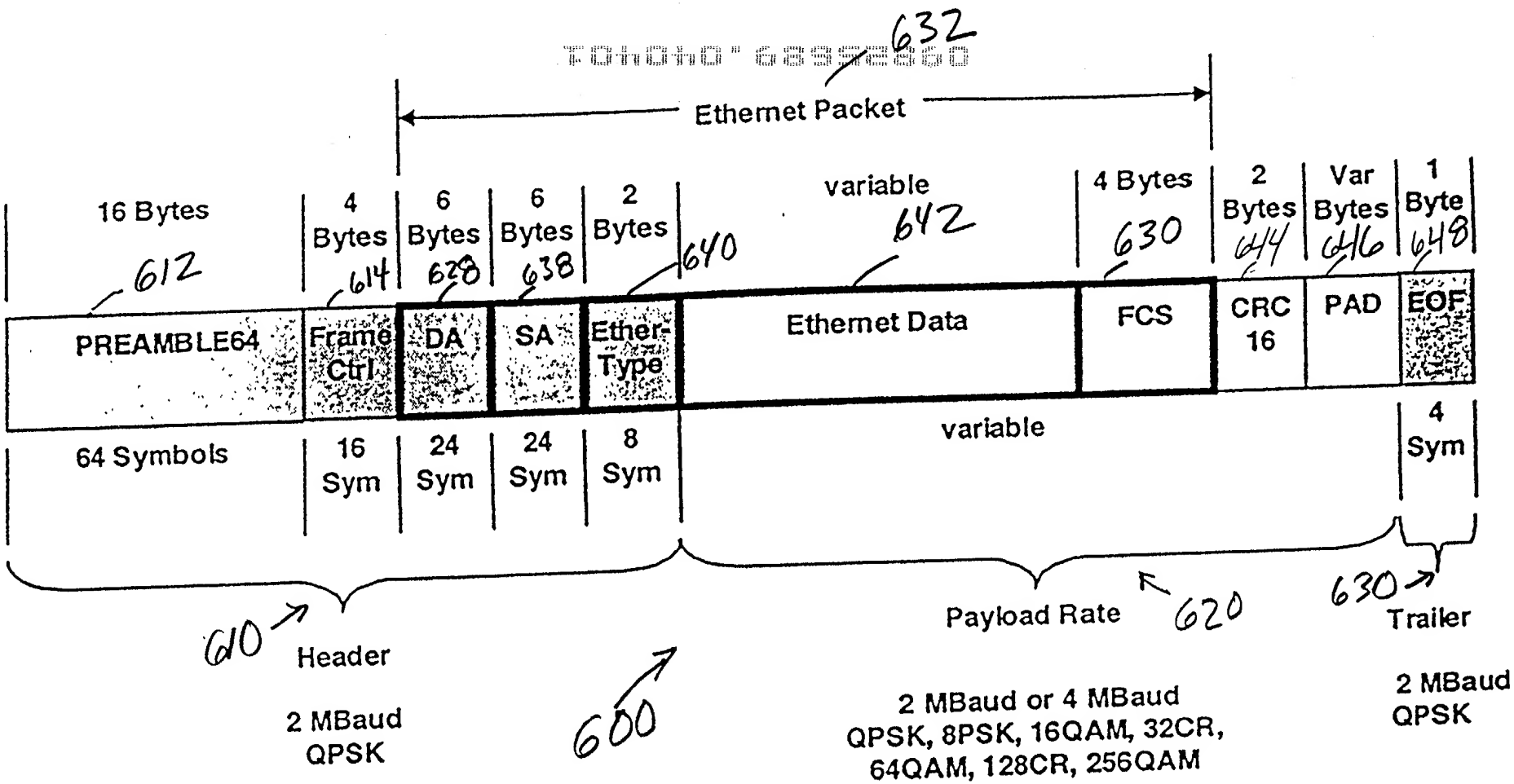

Ethernet Packet
16 Bytes
4 Bytes
6 Bytes
6 Bytes
2 Bytes
variable
4 Bytes
2 Bytes
Var Bytes
1 Byte
PREAMBLE64
Frame Ctrl
DA
SA
Ether-Type
Ethernet Data
FCS
CRC 16
PAD
EOF
64 Symbols
16 Sym
24 Sym
24 Sym
8 Sym
variable
4 Sym
Payload Rate
Header
Trailer
2 MBaud QPSK
2 MBaud or 4 MBaud QPSK, 8PSK, 16QAM, 32CR, 64QAM, 128CR, 256QAM
2 MBaud QPSK
= 4 Mbaud only

FIG. 6

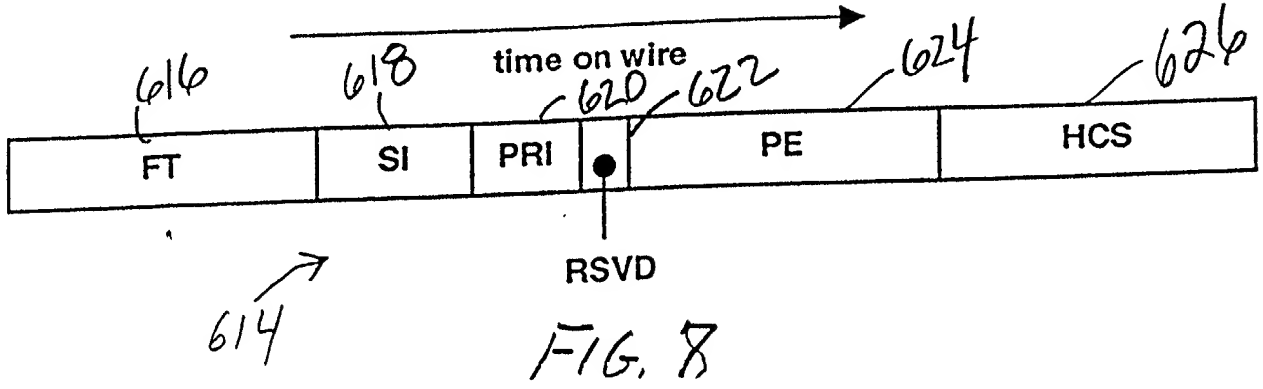

time on wire
FT
SI
PRI
RSVD
PE
HCS

FIG. 8

Field	Bit Number	Bits	Description
FT	31:24	8	Frame Type. This field shall be set to zero by the transmitter. The receiver shall decode this field and discard the frame if it's anything other than zero.
RSVD	23	1	Reserved. This field shall be set to zero by the transmitter, and the receiver shall ignore it
PRI	22:20	3	Priority (0-7)
SI	19:16	4	Scrambler Initialization
PE	15:8	8	Payload Encoding
HCS	7:0	8	Header Check Sequence

FIG. 7

Value	Interpretation
0	Reserved on transmit, discard frame on receive
1	Baud rate=2 MHz, 2 bits per Baud
2	Baud rate=2 MHz, 3 bits per Baud
3	Baud rate=2 MHz, 4 bits per Baud
4	Baud rate=2 MHz, 5 bits per Baud
5	Baud rate=2 MHz, 6 bits per Baud
6	Baud rate=2 MHz, 7 bits per Baud
7	Baud rate=2 MHz, 8 bits per Baud
8	Reserved on transmit, discard frame on receive
9	Baud rate=4 MHz, 2 bits per Baud
10	Baud rate=4 MHz, 3 bits per Baud
11	Baud rate=4 MHz, 4 bits per Baud
12	Baud rate=4 MHz, 5 bits per Baud
13	Baud rate=4 MHz, 6 bits per Baud
14	Baud rate=4 MHz, 7 bits per Baud
15	Baud rate=4 MHz, 8 bits per Baud
16-256	Reserved on transmit, discard frame on receive

FIG. 9

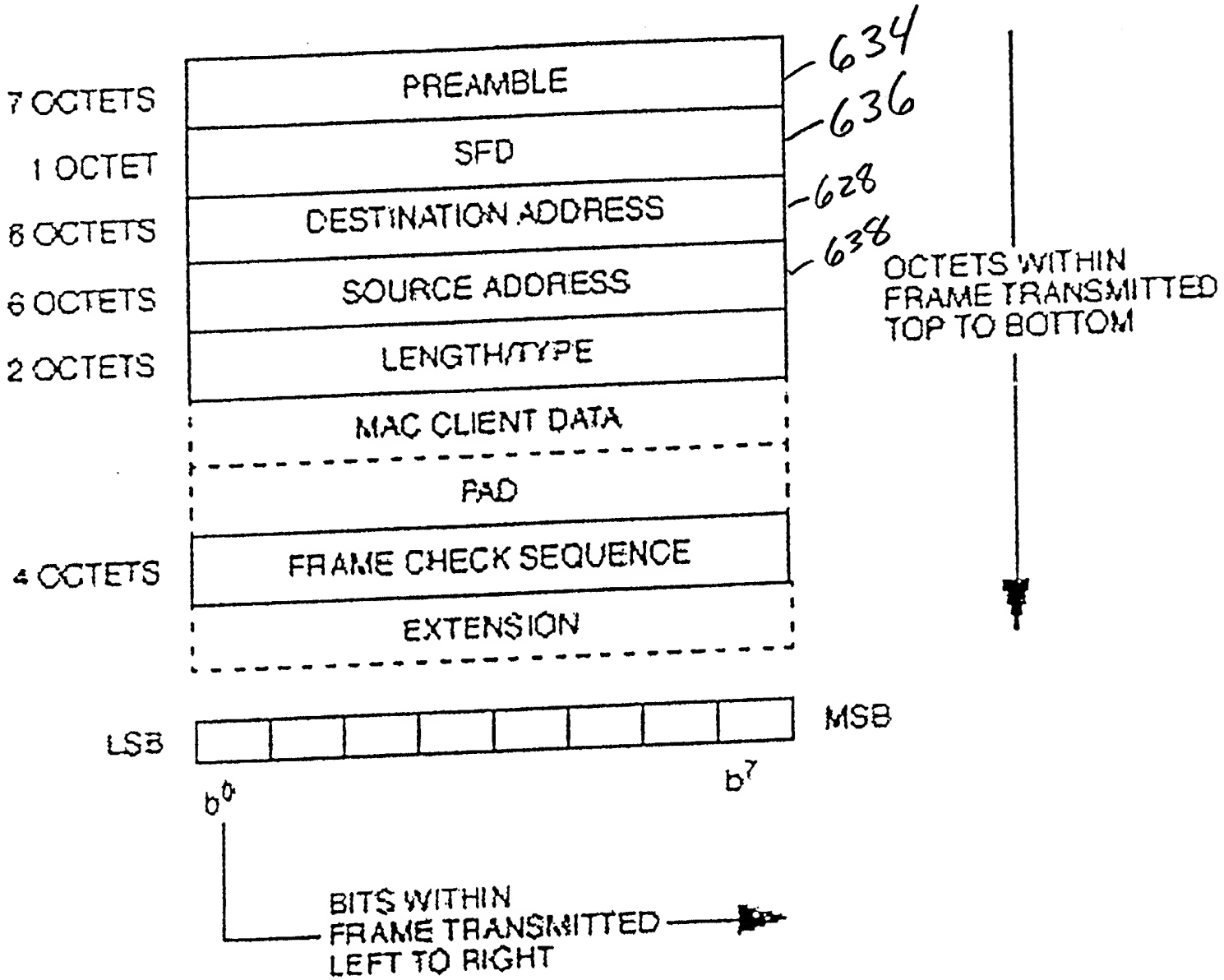

7 OCTETS
PREAMBLE
1 OCTET
SFD
6 OCTETS
DESTINATION ADDRESS
6 OCTETS
SOURCE ADDRESS
2 OCTETS
LENGTH/TYPE
MAC CLIENT DATA
PAD
4 OCTETS
FRAME CHECK SEQUENCE
EXTENSION
634
636
628
638
OCTETS WITHIN FRAME TRANSMITTED TOP TO BOTTOM
LSB
MSB
b0
b7
BITS WITHIN FRAME TRANSMITTED LEFT TO RIGHT

FIG. 10

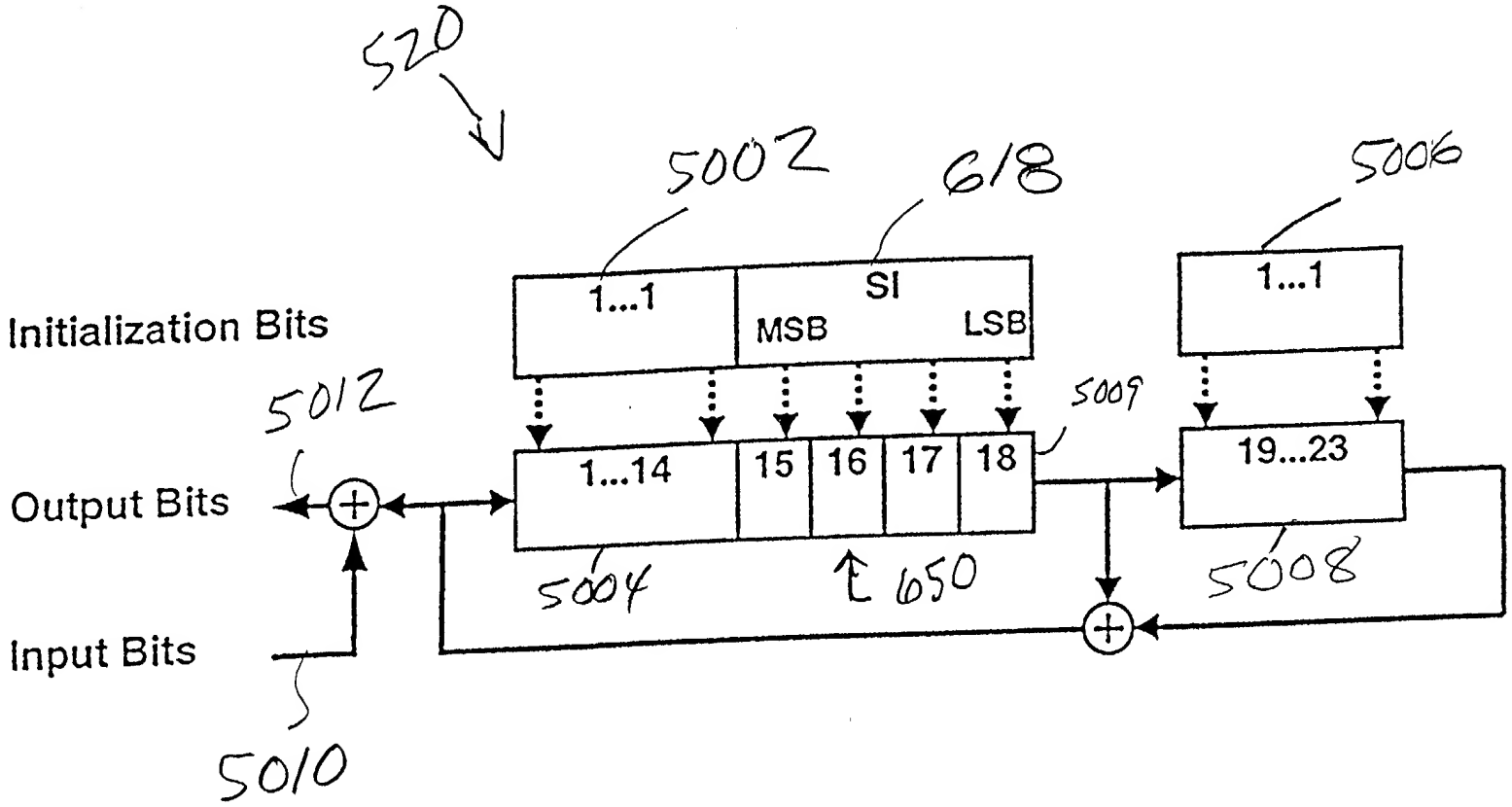


FIG. 11

2 bits per Baud

FIG 12a →

01	00
11	10

3 bits per Baud

FIG 12b →

	011	001	
010			000
110			100
	111	101	

4 bits per Baud

FIG 12c →

0111	0110	0010	0011
0101	0100	0000	0001
1101	1100	1000	1001
1111	1110	1010	1011

5 bits per Baud

FIG 12d →

	01010	01110	00110	00010	
01111	01101	01100	00100	00101	00111
01011	01001	01000	00000	00001	00011
11011	11001	11000	10000	10001	10011
11111	11101	11100	10100	10101	10111
	11010	11110	10110	10010	

6 bits per Baud

011010	011011	011001	011000	001000	001001	001011	001010
011110	011111	011101	011100	001100	001101	001111	001110
010110	010111	010101	010100	000100	000101	000111	000110
010010	010011	010001	010000	000000	000001	000011	000010
110010	110011	110001	110000	100000	100001	100011	100010
110110	110111	110101	110100	100100	100101	100111	100110
111110	111111	111101	111100	101100	101101	101111	101110
111010	111011	111001	111000	101000	101001	101011	101010

FIG 12e →

7 BITS PER BAUD

			0101100	0101101	0111101	0111100	0011100	0011101	0001101	0001100	
			0100100	0100101	0110101	0110100	0010100	0010101	0000101	0000100	
0110111	0110110	0110010	0110011	0110001	0110000	0010000	0010001	0010011	0010010	0010110	0010111
0111111	0111110	0111010	0111011	0111001	0111000	0011000	0011001	0011011	0011010	0011110	0011111
0101111	0101110	0101010	0101011	0101001	0101000	0001000	0001001	0001011	0001010	0001110	0001111
0100111	0100110	0100010	0100011	0100001	0100000	0000000	0000001	0000011	0000010	0000110	0000111
1100111	1100110	1100010	1100011	1100001	1100000	1000000	1000001	1000011	1000010	1000110	1000111
1101111	1101110	1101010	1101011	1101001	1101000	1001000	1001001	1001011	1001010	1001110	1001111
1111111	1111110	1111010	1111011	1111001	1111000	1011000	1011001	1011011	1011010	1011110	1011111
1110111	1110110	1110010	1110011	1110001	1110000	1010000	1010001	1010011	1010010	1010110	1010111
			1100100	1100101	1110101	1110100	1010100	1010101	1000101	1000100	
			1101100	1101101	1111101	1111100	1011100	1011101	1001101	1001100	

FIG. 12f →

8 BITS PER BAUD

FIG. 12g

Bits per Baud	Reference Point(s)	Value
2	00	1+i
3	000	(12+5i)/9
	001	(5+12i)/9
4	0000	(1+i)/3
5	00000	(1+i)/4
6	000000	(1+i)/7
7	0000000	(1+i)/9
8	00000000	(1+i)/15

FIG. 13

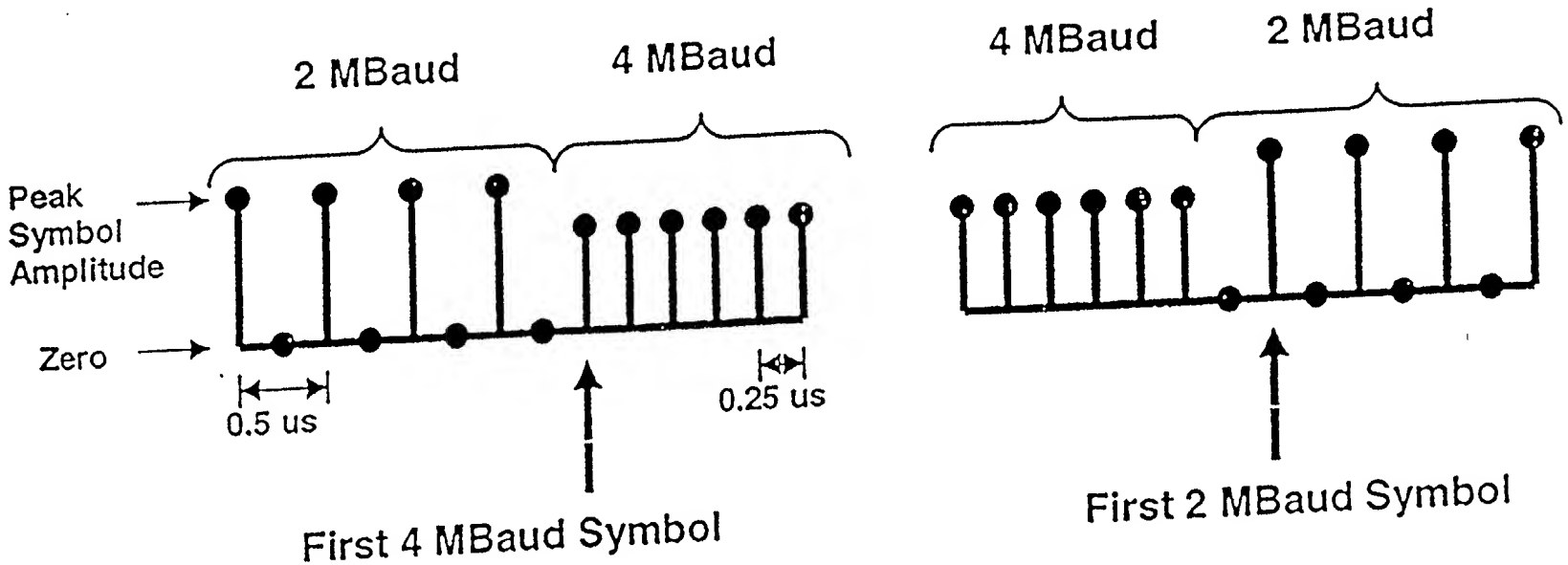


FIG. 14

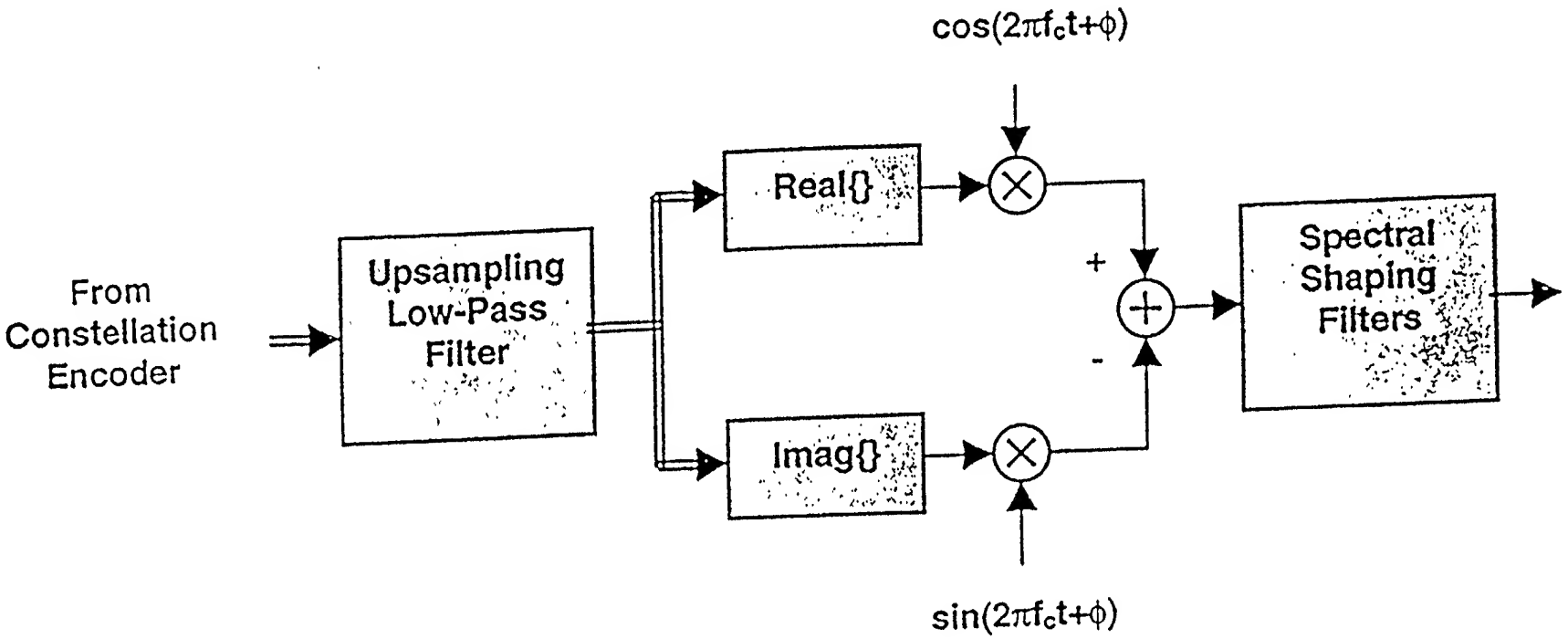

cos(2πf_ct+φ)
From Constellation Encoder
Upsampling Low-Pass Filter
Real{}
Imag{}
+
-
Spectral Shaping Filters
sin(2πf_ct+φ)

FIG. 15

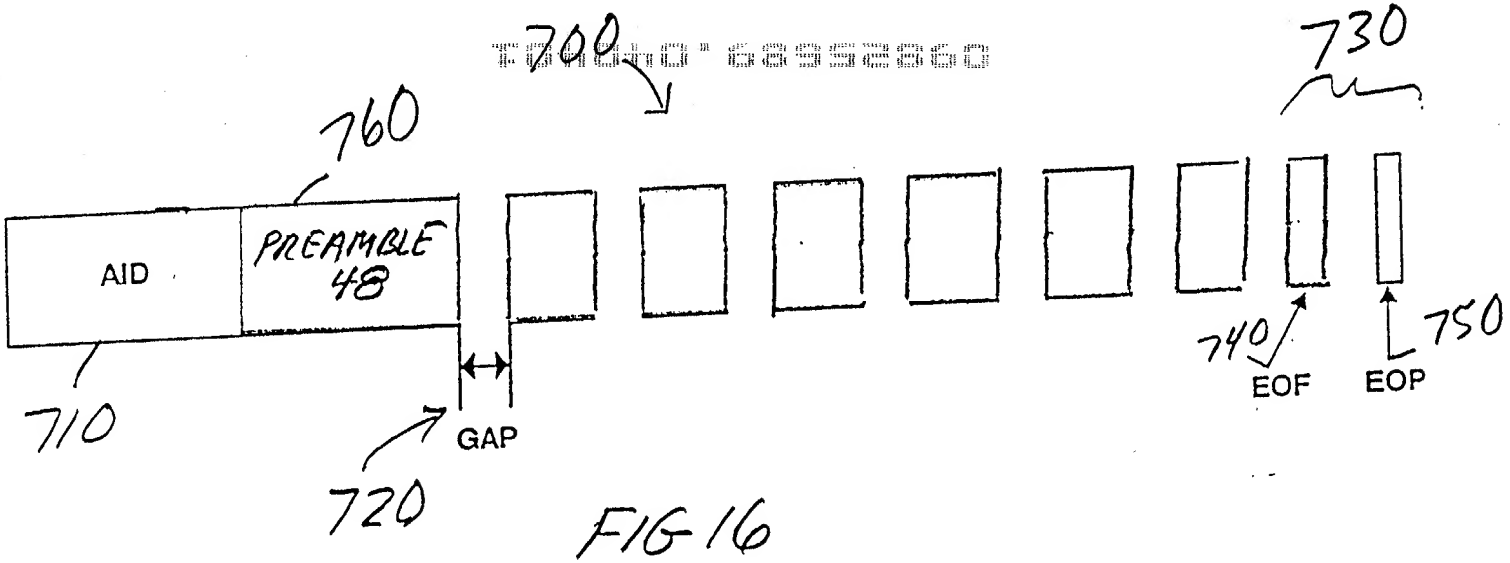

700
730
760
AID
PREAMBLE
48
710
GAP
720
740
EOF
EOP
750

FIG 16

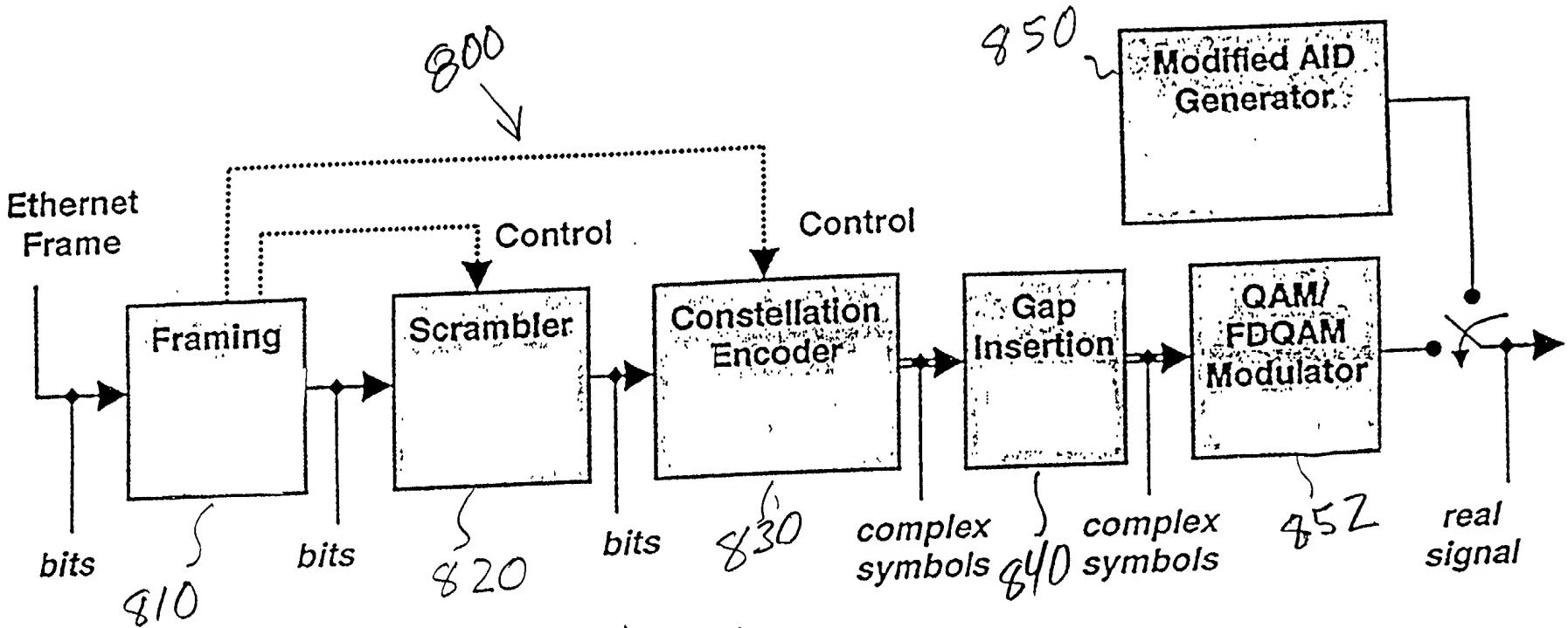

800
850
Modified AID Generator
Ethernet Frame
Control
Control
Framing
Scrambler
Constellation Encoder
Gap Insertion
QAM/ FDQAM Modulator
bits
bits
bits
complex symbols
complex symbols
real signal
810
820
830
840
852

FIG 17

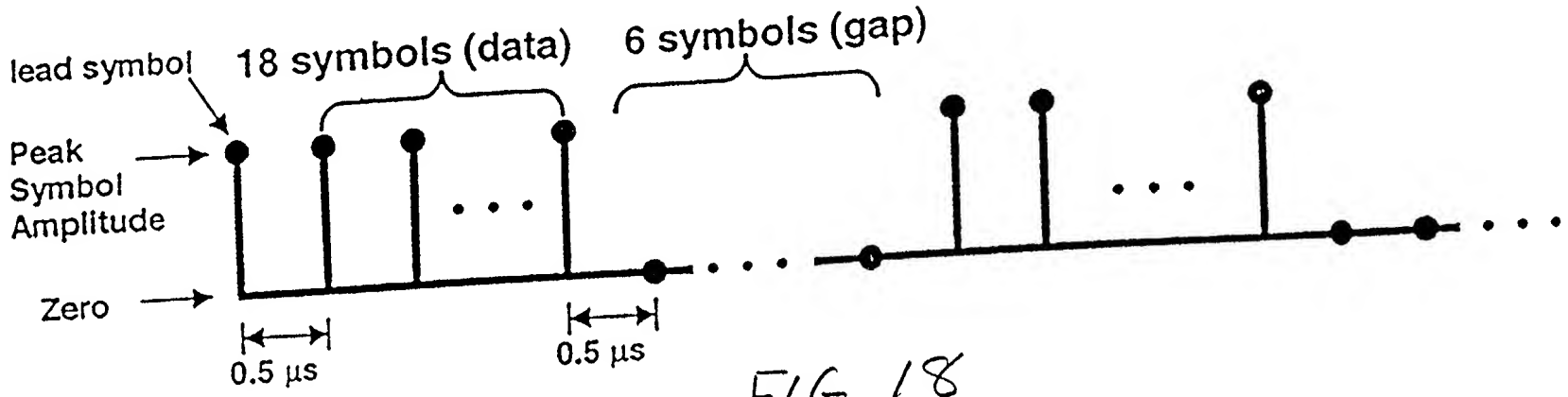

lead symbol
18 symbols (data)
6 symbols (gap)
Peak
Symbol
Amplitude
Zero
0.5 µs
0.5 µs

FIG. 18

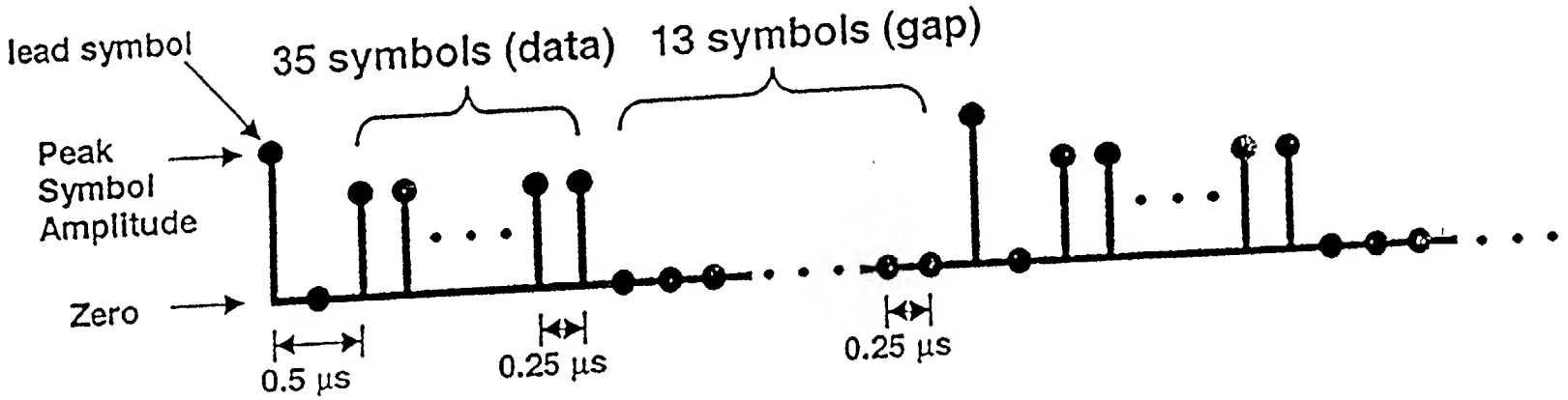

lead symbol
35 symbols (data)
13 symbols (gap)
Peak
Symbol
Amplitude
Zero
0.5 µs
0.25 µs
0.25 µs

FIG. 19

M *modulo* 2	P *modulo* 2	EOF/EOP sequence
0	0	• 4 symbols, defined by the bits 0xfc • 12 zero symbols • 1 symbol, defined by the bits 00
0	1	• 4 symbols, defined by the bits 0x03 • 12 zero symbols • 1 symbol, defined by the bits 11
1	0	• 4 symbols, defined by the bits 0x03 • 12 zero symbols • 1 symbol, defined by the bits 11
1	1	• 4 symbols, defined by the bits 0xfc • 12 zero symbols • 1 symbol, defined by the bits 00

FIG. 20

M *modulo* 2	P *modulo* 4	EOF/EOP sequence
0	0	• 4 symbols, defined by the bits 0xfc • 12 zero symbols • 1 symbol, defined by the bits 00
0	1	• 4 symbols, defined by the bits 0x56 • 12 zero symbols • 1 symbol, defined by the bits 10
0	2	• 4 symbols, defined by the bits 0x03 • 12 zero symbols • 1 symbol, defined by the bits 11
0	3	• 4 symbols, defined by the bits 0xa9 • 12 zero symbols • 1 symbol, defined by the bits 01
1	0	• 4 symbols, defined by the bits 0x03 • 12 zero symbols • 1 symbol, defined by the bits, 11
1	1	• 4 symbols, defined by the bits 0xa9 • 12 zero symbols • 1 symbol, defined by the bits 01
1	2	• 4 symbols, defined by the bits 0xfc • 12 zero symbols • 1 symbol, defined by the bits 00
1	3	• 4 symbols, defined by the bits 0x56 • 12 zero symbols • 1 symbol, defined by the bits 10

FIG. 21

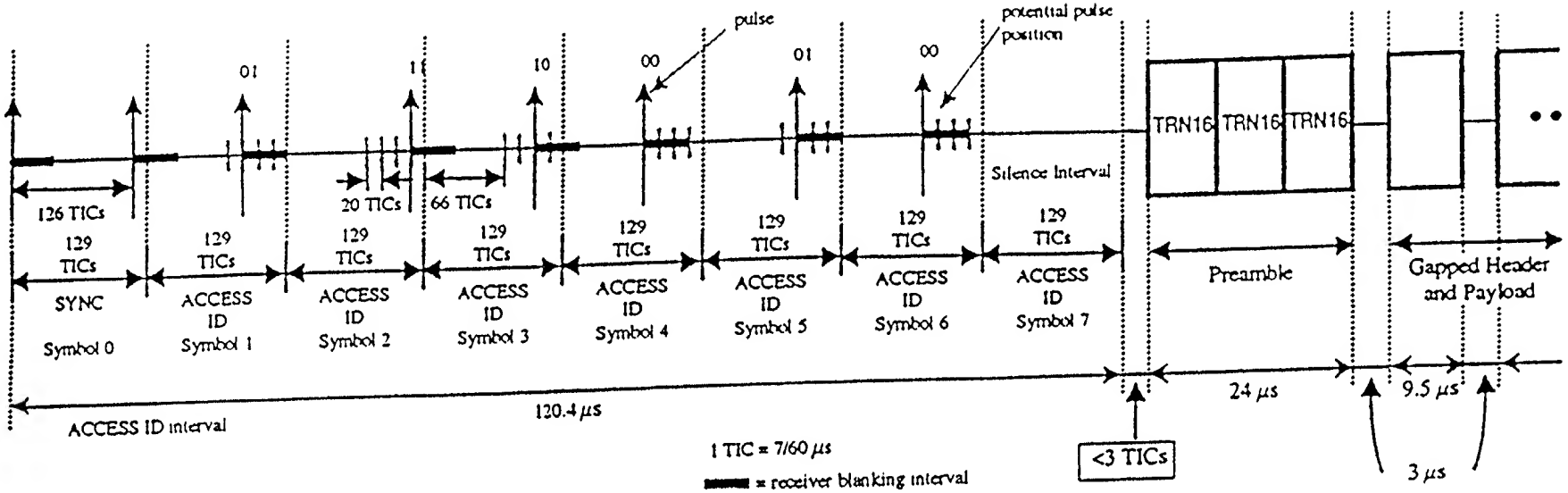

pulse
potential pulse position
01
11
10
00
01
00
TRN16
TRN16
TRN16
126 TICs
20 TICs
66 TICs
Silence Interval
129 TICs
SYNC
Symbol 0
ACCESS ID Symbol 1
ACCESS ID Symbol 2
ACCESS ID Symbol 3
ACCESS ID Symbol 4
ACCESS ID Symbol 5
ACCESS ID Symbol 6
ACCESS ID Symbol 7
Preamble
Gapped Header and Payload
ACCESS ID interval
120.4 μs
24 μs
9.5 μs
3 μs
1 TIC = 7/60 μs
= receiver blanking interval
<3 TICs

FIG. 22

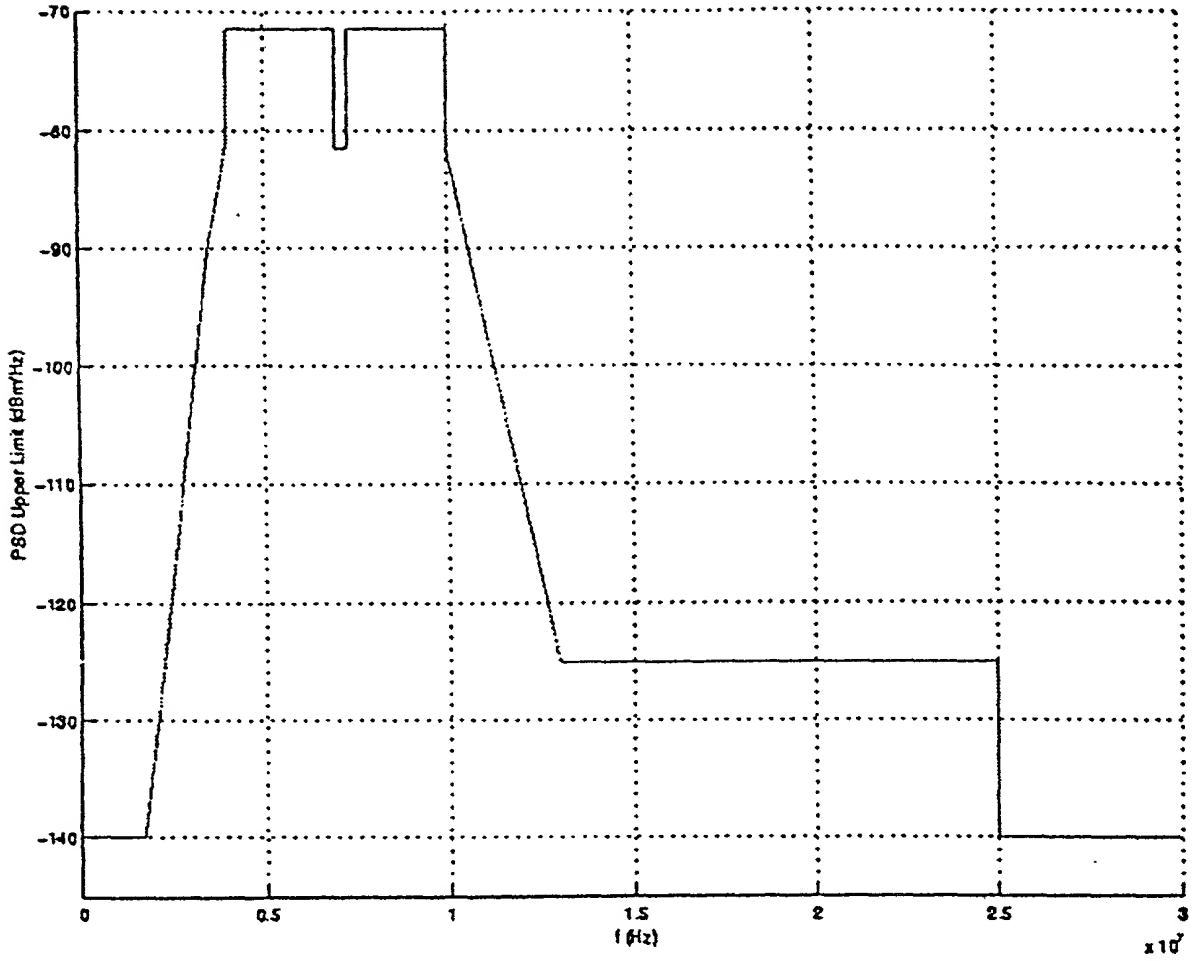


FIG. 23a

Frequency (MHz)	PSD Limit (dBm/Hz)
0.015 < f <= 1.7	-140
1.7 < f <= 3.5	-140 + (f – 1.7)*50.0/1.8
3.5 < f <= 4.0	-90 + (f – 3.5)*17.0
4.0 < f < 7.0	-71.5
7.0 <= f <= 7.3	-81.5
7.3 < f < 10.0	-71.5
10.0 <= f < 13.0	-81.5 – (f –10.0)*43.5/3.0
13.0 <= f < 25.0	-125
25.0 <= f < 30.0	-140

FIG. 23b

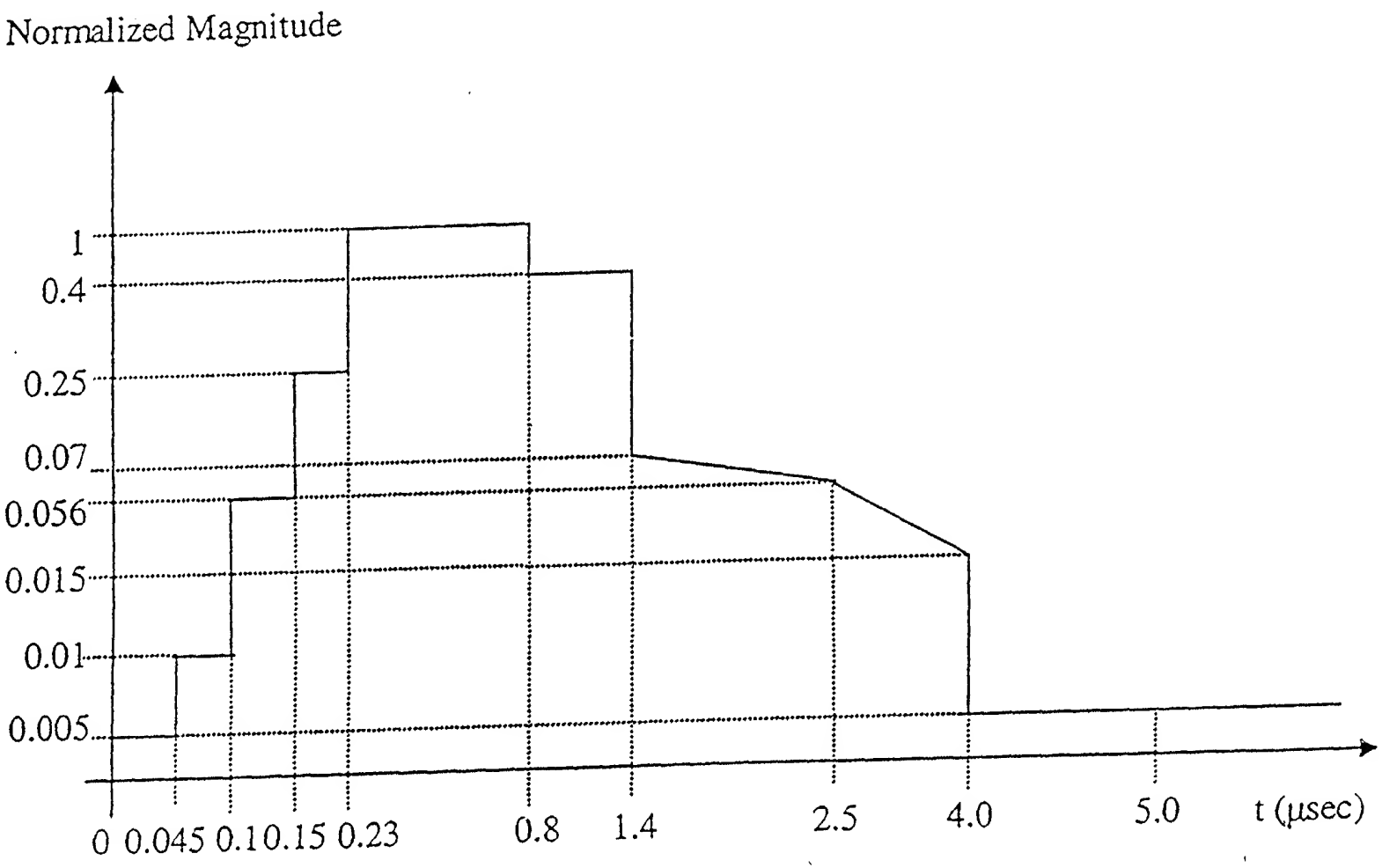

Normalized Magnitude
1
0.4
0.25
0.07
0.056
0.015
0.01
0.005
0 0.045 0.10.15 0.23
0.8
1.4
2.5
4.0
5.0
t (μsec)

FIG. 24

Frequency Range (MHz)	Maximum Peak-to-PeakInterferer Level (Volts)
0.01 – 0.1	6.0
0.1 – 0.6	3.3
0.6 – 1.7	1.0
1.7 – 4.0	0.1
7.0 – 7.3	0.1
10.0 – 10.15	0.1
14.0 – 14.35	0.28
18.068 – 18.168	0.5
21.0 – 21.45	0.5
24.89 – 24.99	0.5
28.0 – 29.7	0.5

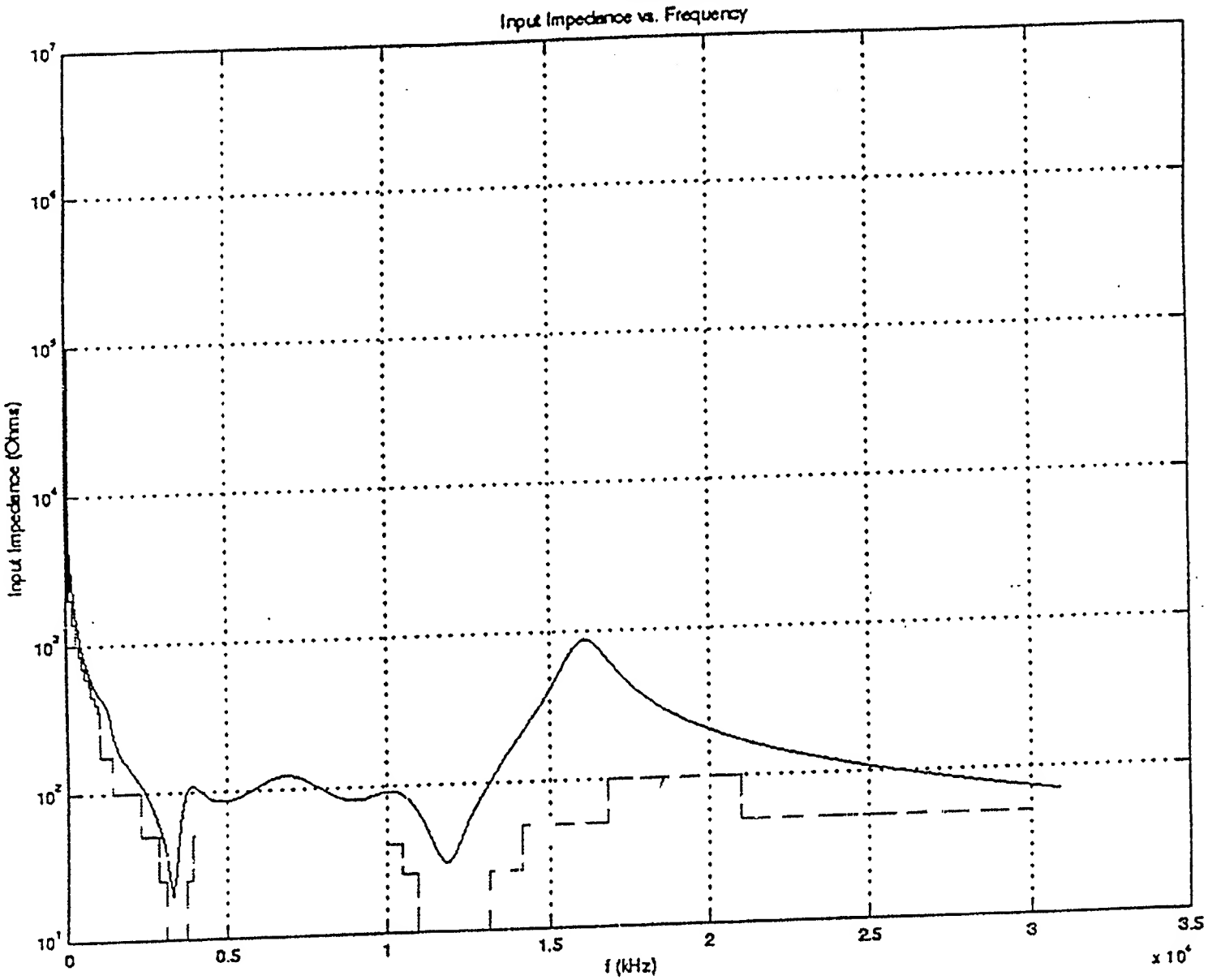
FIG. 25

Frequency Range (MHz)	Maximum Peak-to-PeakInterferer Level (Volts)
0.01 – 0.1	20.0
0.1 – 0.6	20.0
0.6 – 1.7	10.0
1.7 – 4.0	2.5
7.0 – 7.3	2.5
10.0 – 10.15	2.5
14.0 – 14.35	5.0
18.068 – 18.168	5.0
21.0 – 21.45	5.0
24.89 – 24.99	5.0
28.0 – 29.7	5.0

FIG. 26

Frequency Range (kHz)	Min. Impedance (Ohms)
0 < f <= 0.285	1 M
0.285 < f <= 2.85	100 k
2.85 < f <= 28.5	10 k
28.5 < f <= 95	4.0 k
95 < f <= 190	2.0 k
190 < f <= 285	1.4 k
285 < f <= 380	1.0 k
380 < f <= 475	850
475 < f <= 570	700
570 < f <= 665	600
665 < f <= 760	525
760 < f <= 855	450
855 < f <= 950	400
950 < f <= 1000	350
1000 < f <= 1400	175
1400 < f <= 2300	100
2300 < f <= 2850	50
2850 < f <= 3085	25
3085 < f <= 3725	10
3725 < f <= 3935	25
3935 < f <= 4000	50
10000 < f <= 10450	40
10450 < f <= 10925	25
10925 < f <= 13125	10
13125 < f <= 14175	25
14175 < f <= 16800	50
16800 < f <= 21000	100
21000 < f <= 30000	50

FIG. 27



— INPUT IMPEDANCE
--- LOWER BOUND MASK

FIG. 28

OSI	IEEE	Function
DATA LINK	–	**Link Layer Signaling (driver)** a) Rate Adaptation, QoS and 1M8 Compatibility b) LARQ Error Recovery c) Link Integrity and Capability Discovery
	MAC Controller Layer	**MAC Controller Layer Functions** a) Host Interface b) Control and Status Registers, Interrupts c) DMA transfers, data buffering and command list interpretation d) Performance counters e) MAC address filtering, Wake-On-LAN processing
	MII	**Optional MII Interface (in PHY-only)**
	LLC – Logical Link Control	**Optional Link Layer Signaling (in PHY-only)** a) Rate Adaptation, QoS and 1M8 Compatibility b) c) Link Integrity and Capability Discovery
		Frame Processing (transmit and receive) a) Framing (frame boundary delineation and synchronization) b) Error detection (FCS generation and check, fragment detection)
	V2 MAC	**Media Access Control (MAC)** a) CSMA/CD b) Collision Resolution (backoff algorithm)
PHY	PHY	**Physical Coding Sublayer** a) Coding and Modulation, Carrier Sense, Collision Detection

FIG. 29

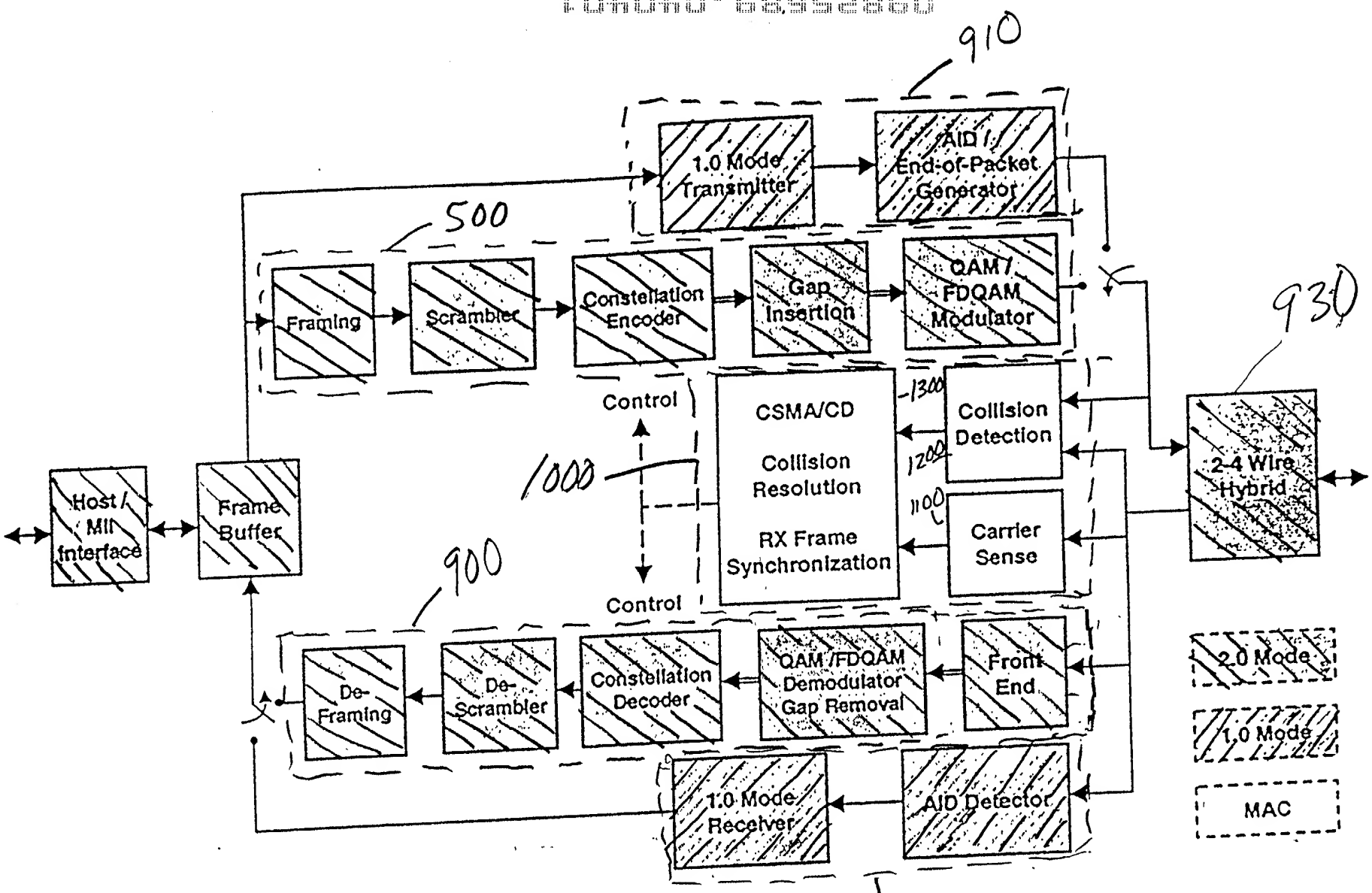

910
1.0 Mode Transmitter
AID / End-of-Packet Generator
500
Framing
Scrambler
Constellation Encoder
Gap Insertion
QAM / FDQAM Modulator
930
Control
CSMA/CD
Collision Resolution
RX Frame Synchronization
1300
Collision Detection
1200
1100
Carrier Sense
2-4 Wire Hybrid
1000
Host / MII Interface
Frame Buffer
900
Control
De-Framing
De-Scrambler
Constellation Decoder
QAM / FDQAM Demodulator Gap Removal
Front End
2.0 Mode
1.0 Mode
MAC
1.0 Mode Receiver
AID Detector
920

FIG. 30

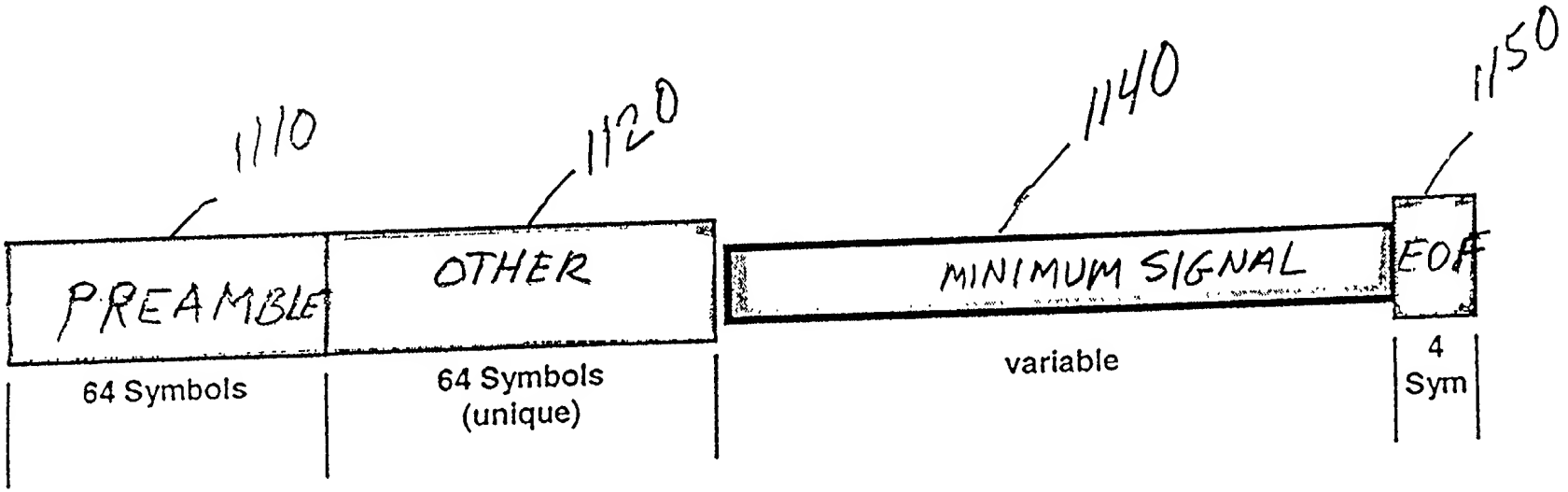

1110
1120
1140
1150
PREAMBLE
OTHER
MINIMUM SIGNAL
EOF
64 Symbols
64 Symbols
(unique)
variable
4
Sym

FIG. 31

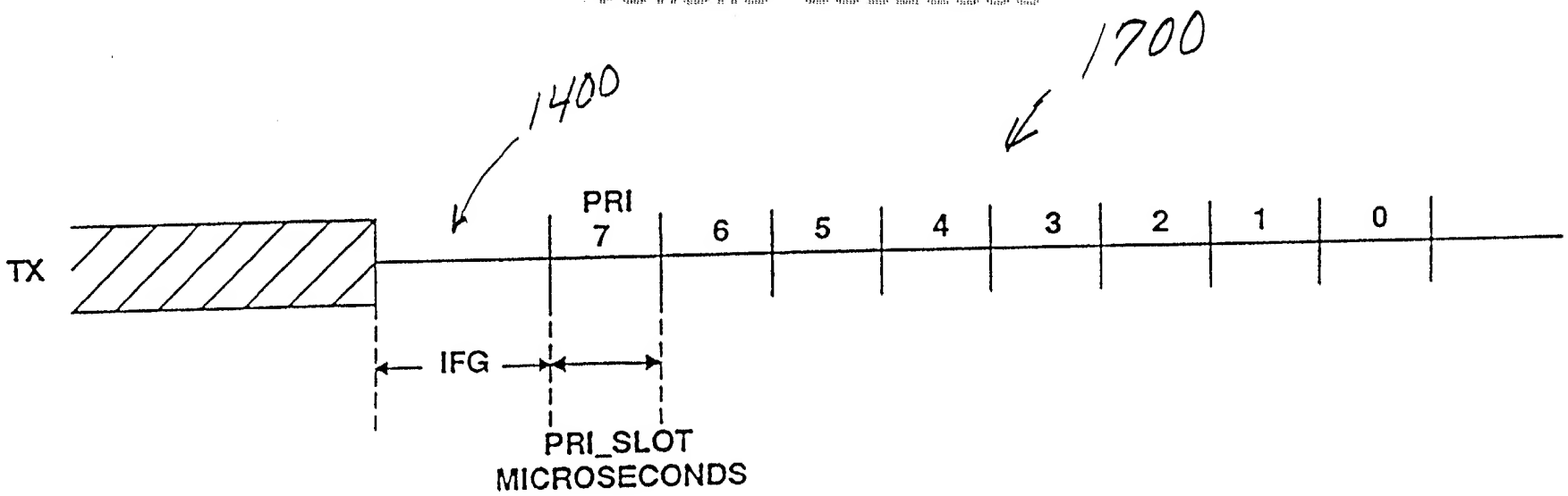

1700
1400
PRI
7
6
5
4
3
2
1
0
TX
IFG
PRI_SLOT
MICROSECONDS

FIG. 32

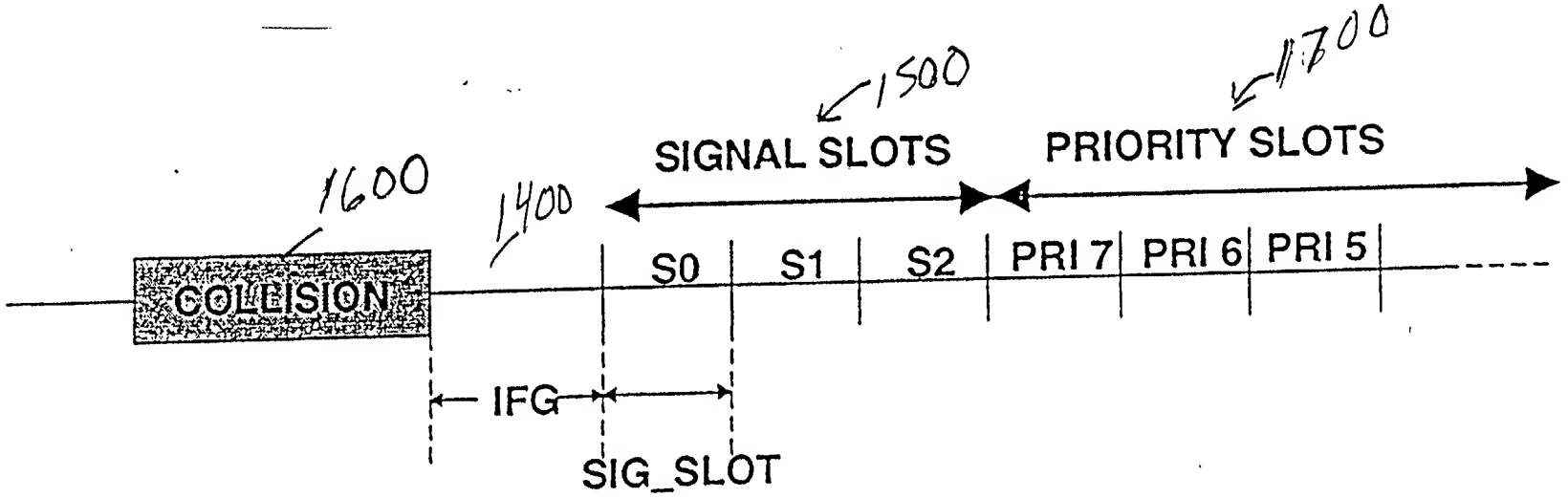

1700
1500
SIGNAL SLOTS
PRIORITY SLOTS
1600
1400
COLLISION
S0
S1
S2
PRI 7
PRI 6
PRI 5
IFG
SIG_SLOT

FIG. 33

Without Priority Access:

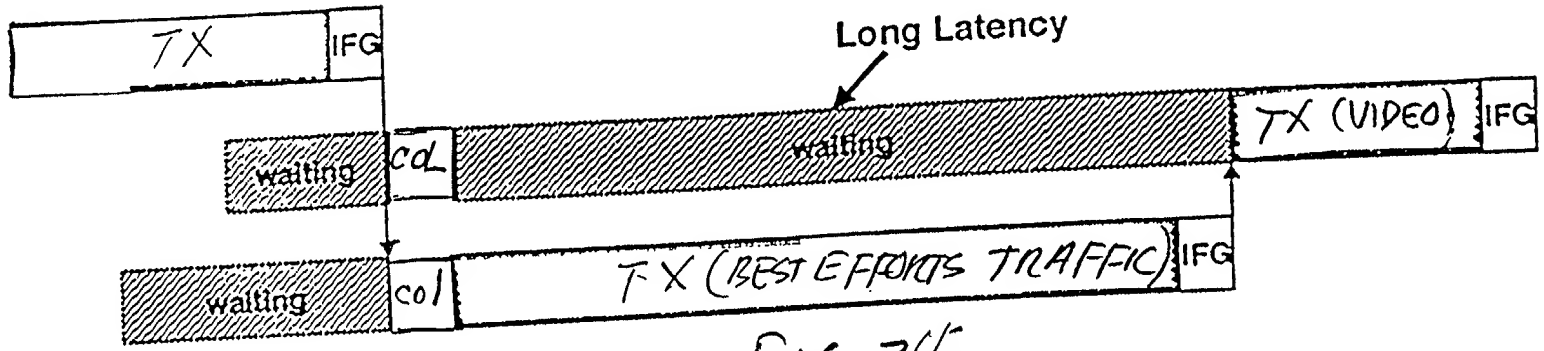


FIG. 34a

With Priority Access:

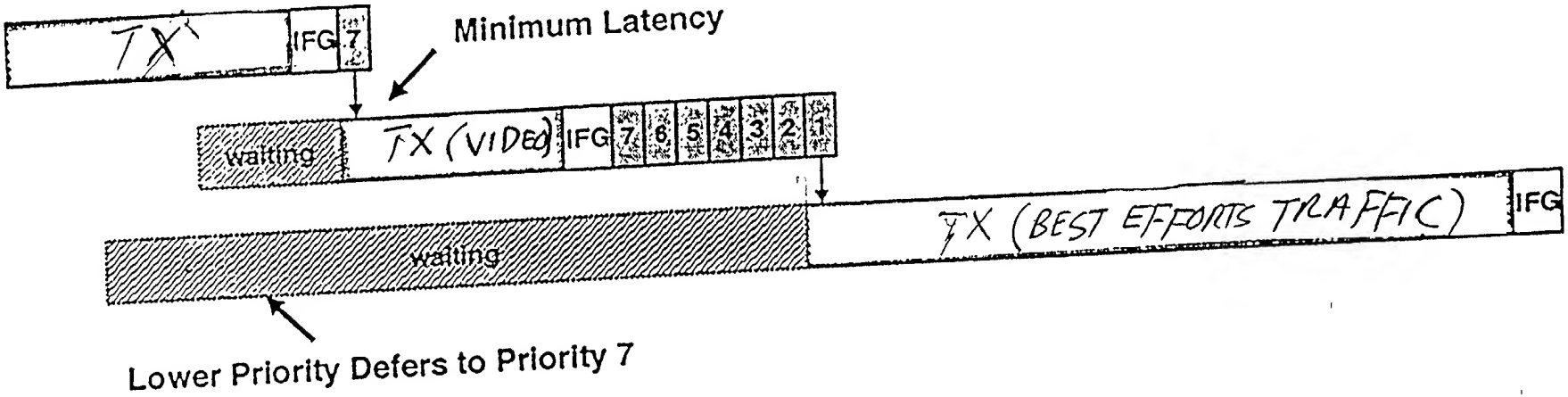


FIG. 34b

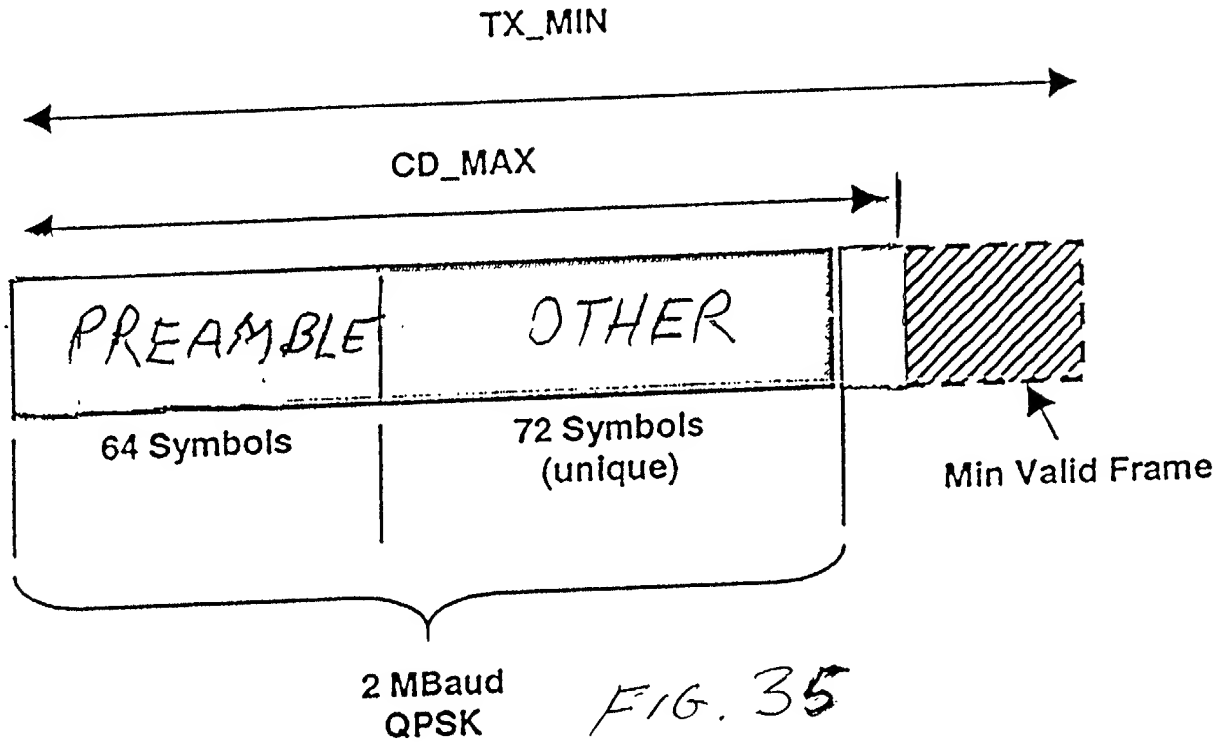

TX_MIN
CD_MAX
PREAMBLE
OTHER
64 Symbols
72 Symbols
(unique)
Min Valid Frame
2 MBaud
QPSK

FIG. 35

Section	Parameter	Min	Max	Units
Basic CSMA	NOMINAL_RMS_VOLTAGE	100	–	mVrms
	CS_RANGE	38	–	dB
	CS_IFG	29.0-Δ	29.0+Δ	microseconds
	CS_DEFER	–	12.0	microseconds
	minFrameSize	64	–	octets
	maxFrameSize	1526	See 3.3.7.1	octets
	TX_FRAME	92.5	See 3.3.7.1	microseconds
	TX_ON	0	4.0	microseconds
Priority Access	PRI_SLOT	21.0-Δ	21.0+Δ	microseconds
Collision Detection	CD_FRAG	70.0-Δ	70.0+Δ	microseconds
	CD_MIN	32.0	–	microseconds
	CD_THRESHOLD (recommended)	–	92.0	microseconds
	CD_RANGE	36	–	dB
	CD_OFFSET_EARLY	–	12.0	microseconds
	CD_OFFSET_LATE	–	15.0	microseconds
Collision Resolution	attemptLimit	256	256	
	SIG_SLOT	32.0-Δ	32.0+Δ	microseconds

FIG. 36

Field	Length	Explanation
DA	6 octets	Destination Address
SA	6 octets	Source Address
Ethertype	2 octets	0x886c (Link Protocol Frame. Assigned to ASSIGNED by IEEE)
SSType	1 octet	0 – Reserved 1 – Rate Request Control Frame 2 – Link Integrity Short Frame 3 – Capabilities Announcement 4 – LARQ 5 – Vendor-specific short format type 6 –126 Reserved 127 Reserved Values 128-255 correspond to the Long Subtype
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field (or the first octet following SSLength if it is not defined as SSVersion) and ending with the second(last) octet of the Next Ethertype field. Min is 2 and max is 255.
SSVersion	1 octet	Version number of the control information
Data	0-252 octets	Control information
Next Ethertype	2 octets	Ethertype/length of next layer protocol, 0 if none.
Pad	41-0 octets	Padding required to meet minimum if data < 41 octets
FCS	4 octets	Frame Check Sequence

FIG, 37

Field	Length	Explanation
DA	6 octets	Destination Address
SA	6 octets	Source Address
Ethertype	2 octets	0x886c (Link Protocol Frame. Assigned to Epigram by IEEE)
LSType	2 octets	32768 Reserved 32769 Vendor-specific long-format 32770 - 65534 reserved 65535 Reserved
LSLength	2 octets	Number of additional octets in the control header, starting with the SSVersion field (or the first octet following SSLength if it is not defined as SSVersion) and ending with the second(last) octet of the Next Ethertype field. Min is 2 and max is 65535.
LSVersion	1 octet	Version number of the following protocol information
Data	LSLength - 3 octets	LSType protocol dependent data
Next Ethertype	2 octets	Ethertype/length of next layer protocol, 0 if none.
Pad	42-0 octets	pad to minimum size if needed
FCS	4 octets	Frame Check Sequence

FIG. 38

Field	Length	Meaning
DA	6 octets	Destination Address
SA	6 octets	Source Address
Ethertype	2 octets	**0x886c** (Link Control Frame)
SSType	1 octet	=1
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field and ending with the second(last) octet of the Next Ethertype field. The minimum value of SSLength is 8 for SSVersion 0.
SSVersion	1 octet	=0
OpCode	1 octet	Operation code for this control message.
NumBands	1 octet	Number of bands specified in this control. Each band has a two octet descriptor. The first band refers to 2 MBaud modulation rate, the next to 4 MBaud. NumBands shall be 1 or 2 on transmission for 10M8 stations, and stations shall ignore band entries beyond Band2 on receive if NumBands is larger than 2. The value 0 is not allowed.
NumAddr	1 octet	Number of addresses specified in the payload of this control message. NumAddr may be zero. The SA in the Ethernet header is always used, and is referred to in the following sections as RefAddr0.
Band1_PE	1 octet	2MBaud, 7 MHz carrier : The PE value that should be used to send data when the 2MBaud band is selected. (1..8) are the only valid values. The value 8 is used to request HPNA 1.0 type frames, and is valid only when the network is operating in V1M2mode, and only in Band1.
Band1_rank	1 octet	The rank order of the ReqDAs' preference for this band, 1 is highest preference, and the other bands are assigned successively larger rank values, no two bands shall have the same rank
Band2_PE	1 octet	Optional, only present if NumBands >= 2. 4MBaud, 7 MHz carrier. If included, this field is the PE value that should be used to send data when the 4MBaud band is selected. (0, 9..15) are the only valid values.
Band2_rank	1 octet	Optional, only present if NumBands >= 2. Rank order of ReqDAs' preference for this band
RefAddr1	6 octets	Optional. Present if NumAddr >= 1.The second MAC Address for which the rates are being specified, typically Broadcast or a multicast address.
RefAddr2	6 octets	Optional. Present if NumAddr >= 2.The third MAC Address for which the rates are being specified.
...		[additional instances of RefAddr, until the number of RefAddr fields equals NumAddr]
Next Ethertype	2 octets	=0.
Pad		To reach minFrameSize if required
FCS	4 octets	Frame Check Sequence

FIG. 39

PE	Data Rate	Meaning
0	N/A	Means this band is Not Supported
1	4 Mbit/s	2 Mbaud FDQAM, 2 bits per Baud
2	6 Mbit/s	2 Mbaud FDQAM, 3 bits per Baud
3	8 Mbit/s	2 Mbaud FDQAM, 4 bits per Baud
4	10 Mbit/s	2 Mbaud FDQAM, 5 bits per Baud
5	12 Mbit/s	2 Mbaud FDQAM, 6 bits per Baud
6	14 Mbit/s	2 Mbaud FDQAM, 7 bits per Baud
7	16 Mbit/s	2 Mbaud FDQAM, 8 bits per Baud
8	1 Mbit/s	HPNA 1.0
9	8 Mbit/s	4 Mbaud QAM, 2 bits per Baud
10	12 Mbit/s	4 Mbaud QAM, 3 bits per Baud
11	16 Mbit/s	4 Mbaud QAM, 4 bits per Baud
12	20 Mbit/s	4 Mbaud QAM, 5 bits per Baud
13	24 Mbit/s	4 Mbaud QAM, 6 bits per Baud
14	28 Mbit/s	4 Mbaud QAM, 7 bits per Baud
15	32 Mbit/s	4 Mbaud QAM, 8 bits per Baud

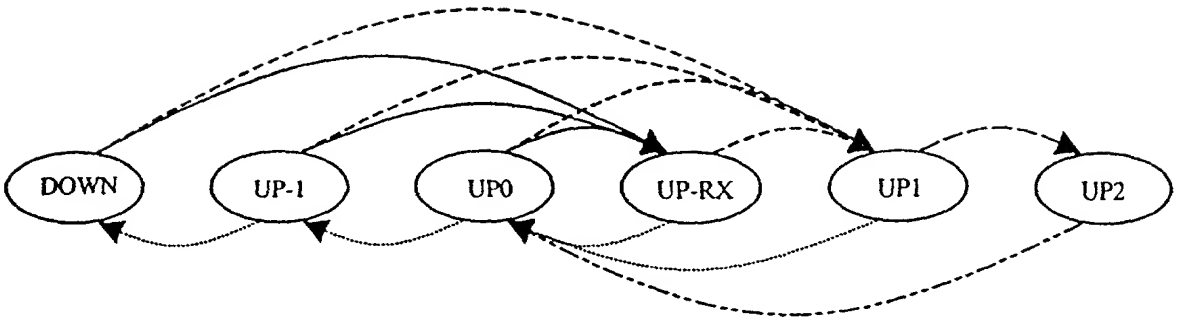
FIG. 40

OpCode	Meaning
0	Rate Change Request
1	Rate Test Request
2	Rate Test Reply
3-255	Reserved

FIG. 41

band specification	A Payload Encoding (PE) and Rank associated with a given band. A band is a single combination of baud rate, modulation type (e.g. QAM or FDQAM) and carrier frequency. Two bands are defined in HPNA V2
Logical channel, channel	A flow of frames from a sender to one or more receivers on a single network segment, consisting of all the frames with a single combination of DA and SA.
Receiver	A station that receives frames sent on a particular channel. If the destination is a unicast address there is at most one receiver. If the destination is a group address (including broadcast), there may be many receivers.
Receiver PE	The preferred PE to be used on this channel, as determined by the receiver.
RRCF	Rate Request Control Frame. Sent from the receiver to the sender to effect a change in PE.
RefAddr0	The SA in the Ethernet header of the RRCF frame. This is the DA of the receiver (for the channel), and is always used by the channel sender as the first RefAddr processed.
RefAddr1..RefAddr<n>	Other addresses including Broadcast and Multicast addresses for which the receiver is indicating rate information to the sender. The channel receiver's station address (RefAddr0) should not be put in the list of additional RefAddr's. Note1: At least one RefAddr field is necessary to support rate negotiation for Broadcast and Multicast addresses since these cannot be used as the source address in the Ethernet header.
Sender	The sending station for a channel, usually the station owning the source MAC address.
Sender PE	The preferred PE associated with a channel, as noted by the sender.

FIG. 42



Receive any non-broadcast frame or link indication

Receive a frame with DA == Broadcast (0xFFFFFFFFFFFF) – **Set SA1 = SA**

Receive a frame with DA == Broadcast (0xFFFFFFFFFFFF) and SA != SA1

Timeout of 1 second free-running timer – **Send LICF, reinitialize Force_Send**

Timeout - If Force_Send == 0 then **Send LICF, reinit Force_Send** else **decrement Force_Send**

FIG. 43a

	DOWN	UP-1	UP0	UP-RX	UP1	UP2
Receive 1.0 link indication or any non-broadcast frame	UP-RX (none)	UP-RX (none)	UP-RX (none)	UP-RX (none)	UP1 (none)	UP2 (none)
Receive broadcast frame with SA == SA1	UP1 Set SA1<-SA	UP1 Set SA1<-SA	UP1 Set SA1<-SA	UP1 Set SA1<-SA	UP1 (none)	UP2 (none)
Receive broadcast frame with SA != SA1	UP1 Set SA1<-SA	UP1 Set SA1<-SA	UP1 Set SA1<-SA	UP1 Set SA1<-SA	Native:UP2 Compat: UP1 (none)	UP2 (none)
Timeout and Force_Send == 0	DOWN Send LICF, reinit Force_Send	DOWN Send LICF, reinit Force_Send	UP-1 Send LICF, reinit Force_Send	UP0 Send LICF, reinit Force_Send	UP0 Send LICF, reinit Force_Send	UP0 Send LICF, reinit Force_Send
Timeout and Force_Send > 0	DOWN Send LICF, reinit Force_Send	DOWN Send LICF, reinit Force_Send	UP-1 Send LICF, reinit Force_Send	UP0 Send LICF, reinit Force_Send	UP0 Send LICF, reinit Force_Send	UP0 decrement Force_Send

FIG. 43b

Field	Length	Meaning
DA	6 octets	Destination Address (FF.FF.FF.FF.FF.FF)
SA	6 octets	Source Address
Ethertype	2 octet	0x886c (Link Control Frame)
SSType	1 octet	=2
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field and ending with the second(last) octet of the Next Ethertype field. Minimum is 4 for SSVersion 0.
SSVersion	1 octet	=0
LI_pad	1 octet	Ignored on reception.
Next Ethertype	2 octets	=0
Pad	41 octets	Any value octet
FCS	4 octets	

FIG. 44

Field	Length	Meaning
DA	6 octets	Destination Address (FF.FF.FF.FF.FF.FF)
SA	6 octets	Source Address of the station that transmitted this frame
Ethertype	2 octet	**0x886c** (Link Control Frame)
SStype	1 octet	=3
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field and ending with the second (last) octet of the Next Ethertype field. Minimum is 32 for SSVersion 0
SSVersion	1 octet	=0
CSA_ID_Space	1 octet	Identifies the registration space of CSA_MFR_ID 0 – Unspecified 1 – JEDEC 2 – PCI
CSA_MFR_ID	2 octets	HW manufacturer ID - Identifies the manufacturer of the PHY controller chip. The purpose of this field plus the part number and revision is to identify specific implementations of the PHY specification. This is not a board or assembly-level identifier.
CSA_Part_No	2 octets	HW Manufacturer Part Number - The part number of the PHY controller chip.
CSA_Rev	1 octet	HW Revision
CSA_Opcode	1 octet	0 – Announce 1 – Request
CSA_MTU	2 octets	Maximum size link-level PDU this receiver accepts in octets, the default value is 1526 octets. This is also the minimum value that shall be accepted by all ILINE10 stations
CSA_SA	6 octets	Source address of the station that generated this CSA frame
CSA_pad	2 octets	Reserved for version 0. Shall be sent as 0, ignored on reception.
CSA_CurrentTxSet	4 octets	Configuration flags, plus all current in-use status for this station.
CSA_OldestTxSet	4 octets	A copy of the "oldest" TX flags for this stations, from the period ending at least one period(minute) earlier.
CSA_CurrentRxSet	4 octets	The union of recent flags received from other stations.
Next Ethertype	2 octets	=0
Pad		Pad to reach minFrameSize if necessary
FCS	4 octets	

FIG. 45

Octet	Field	Length	Description
Flags0	TxPriority7	1	Station is(was) transmitting frames with LL priority 7. (always set)
	TxPriority6	1	Station is(was) transmitting frames with LL priority 6.
	TxPriority5	1	Station is(was) transmitting frames with LL priority 5.
	TxPriority4	1	Station is(was) transmitting frames with LL priority 4.
	TxPriority3	1	Station is(was) transmitting frames with LL priority 3.
	TxPriority2	1	Station is(was) transmitting frames with LL priority 2.
	TxPriority1	1	Station is(was) transmitting frames with LL priority 1.
	TxPriority0	1	Station is(was) transmitting frames with LL priority 0. (always set)
Flags1	Reserved	6	Shall be sent as 0 and ignored by 2.0 stations when received.
	No_V1M2_Frames	1	This station does not support the reception or transmission of compatibility frames (V1M2 frames).
	Supports 4Mbaud	1	This station supports 4 megabaud payload encodings.
Flags2	Reserved	8	Shall be sent as 0 and ignored by 2.0 stations when received.
Flags3	ConfigV2	1	Force use of 10M8 mode, defers to Config1 and ConfigV1M2.
	ConfigV1M2	1	Force use of V1M2 mixed mode, defers to ConfigV1.
	ConfigV1	1	Force use of HPNA 1.x mode, highest precedence of config flags.
	Reserved	2	Shall be sent as 0 and ignored by 2.0 stations when received.
	Highest Version	3	This station's highest supported HPNA version: 0x000 – Reserved 0x001 – HPNA1.0 0x010 – iLine10 0x011-0x111 Reserved

FIG. 46

DeleteSet	A computed value used to detect newly removed status information.
NewRxFlags, ReallyNewRxFlags	Computed values used to detect new status flags.

FIG. 47

CSP_Timer	A free-running timer with a period of 60 seconds.
RetransmitTimer	A one-shot timer, set to a random interval in the range 1 ms to 1000 ms, inclusive, after sending a CSA in which CSA_CurrentTxSet and CSA_OldestTxSet are different, or when a CSA is received with the CSA_Opcode set to 1 (Request). This timer is cancelled if a second CSA is sent as a result of the CSP_Timer expiring.

FIG. 48

NewTxSet	The set of flags announced during the current CS period, updated immediately when a new link layer priority is used or new volatile status is set. When the CSP_Timer expires, CurrentTxSet is given the value of NewTxSet, and NewTxSet is reset to the **default** set.
PreviousTxSet	The set of flags that were announced during the previous CS period (the ending value of NewTxSet from the previous CS period).
OldestTxSet	The set of flags rolled over from PreviousTxSet at the end of the previous CS period (the value of PreviousTxSet from the previous CS period). Flags that are present in OldestTxSet and missing from PreviousTxSet were not actively used or detected (by the sender) for an entire CS period, and will be deleted. This set is sent in CSA frames as CSA_OldestTxSet.
NewRxSet	The union of all CSA_CurrentTxSet flags received in CSAs from other stations during the current CS period. This is rolled over into PreviousRxSet at the expiration of the CSP_Timer, then reset to the empty set (0). A volatile status flag (one of the priority flags) in this set may subsequently be deleted if the only station previously announcing that flag stops using it. The deletion from that station's CurrentTxSet is noted by the difference from its OldestTxSet. The fact that it was the only sender is noted by the absence of the flag in that station's CurrentRxSet, indicating that it has received the flag from no other stations. If deleted from NewRxSet, a flag shall also be deleted from PreviousRxSet.
PreviousRxSet	The set of announced flags received during the previous CS period (the ending value of NewRxSet from the previous CS period). A flag may be deleted from this set, as described under NewRxSet above.

FIG. 49

CurrentTxSet	The set of flags that were announced during the previous CS period plus any new status and priority flags (or changed configuration/options flags) used during the current CS period, i.e. the union of PreviousTxSet and NewTxSet. This set is sent in CSA frames as CSA_CurrentTxSet.
CurrentRxSet	The union of NewRxSet, PreviousRxSet. This set is sent in CSA frames as CSA_CurrentRxSet.
CurrentInUseSet	The union of CurrentTxSet and CurrentRxSet. This set is used to determine the operational mode of the station and to modify the mapping between the LL priority of the frame and the actual PHY priority usage.

FIG. 50

									TX LL priority							
									0	1	2	3	4	5	6	7
CurrentInuse Priorities (any)									Default TX Phy Priorities							
a	n	y	t	x	s	e	t		2	0	1	3	4	5	7	6

FIG. 51a

								TX LL priority							
								0	1	2	3	4	5	6	7
CurrentInuse Priorities (LL)								Remapped TX Phy Priorities							
0							7	6	~~5~~	~~5~~	~~6~~	~~6~~	~~6~~	~~6~~	7
0						6	7	5	~~4~~	~~4~~	~~5~~	~~5~~	~~5~~	7	6
0	1			4			7	5	4	~~4~~	~~5~~	6	~~6~~	~~7~~	7
0			3		5	6	7	3	~~2~~	~~2~~	4	~~4~~	5	7	6

FIG. 51b

Field	Length	Meaning
DA	6 octets	Destination Address
SA	6 octets	Source Address
Ethertype	2 octets	0x886c (Link Control Frame)
SSType	1 octet	=4
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field and ending with the second(last) octet of the Next Ethertype field. SSLength is 6 for SSVersion 0.
SSVersion	1 octet	=0
LARQ_hdr data	3 octets	LARQ Control Header data with LARQ_ctl bit = 1, LARQ_NACK = 0.
Next Ethertype	2 octets	=0
Pad	38 octets	
FCS	4 octets	Frame Check Sequence

FIG. 52a

Field	Length	Meaning
DA	6 octets	Destination Address
SA	6 octets	Source Address
Ethertype	2 octets	0x886c (Link Control Frame)
SSType	1 octet	=4
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field and ending with the second(last) octet of the Next Ethertype field. SSLength is 12 for Nack frames with SSVersion 0.
SSVersion	1 octet	=0
LARQ_hdr data	3 octets	LARQ Control Header data with LARQ_ctl bit = 1, LARQ_NACK = 1..7.
NACK_DA	6 octets	Original Destination Address
Next Ethertype	2 octets	=0
Pad	32 octets	
FCS	4 octets	Frame Check Sequence

FIG. 52b

Field	Length	Meaning
DA	6 octets	Destination Address (from original Ethernet PDU)
SA	6 octets	Source Address (from original Ethernet PDU)
Ethertype	2 octets	0x886c (Link Control Frame)
SStype	1 octet	=4
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field and ending with the second(last) octet of the Next Ethertype field. SSLength is 6 for SSVersion 0.=6
SSVersion	1 octet	=0
LARQ_hdr data	3 octets	LARQ Encapsulation header data (with LARQ_CTL bit = 0)
Next Ethertype	2 octets	From original Ethernet PDU
Payload	Min 46 octets	From original Ethernet PDU payload
FCS	4 octets	Frame Check Sequence

FIG. 52C

Octet	Field	Length	Meaning
Flags0	LARQ_Mult	1 bit	Multiple Retransmission Flag. 0 in the original transmission of a data frame. For retransmitted frames (LARQ_Rtx = 1), set to the value of LARQ_Mult in the NACK frame that caused the retransmission. This flag can be used by receivers to measure the round-trip times associated with the miss/nack/receive-rtx process.
	LARQ_Rtx	1 bit	0 for first transmission of a frame, 1 if frame is retransmitted. Stations not implementing LARQ shall drop any data frame if this bit is 1.
	LARQ_NoRtx	1 bit	0 if implementation supports retransmission, 1 if only priority is meaningful. May be used on a per-channel basis.
	LARQ_NewSeq	1 bit	1 if the sequence number space for the channel has been reset, and older sequence numbers should not be nacked, 0 otherwise
	LARQ_Ctl	1 bit	"0" when in Encapsulation Format
	Priority	3 bits	Link Layer Priority of this frame
Flags1_Seq0	Reserved	4 bits	Reserved, shall be 0
	LARQ_seq_high	4 bits	High 4 bits of Sequence number
Seq1	LARQ_seq_low	8 bits	Low 8 bits of Sequence number

FIG. 52D

Octet	Field	Length	Meaning
Flags0	LARQ_Mult	1 bit	Multiple Retransmission Flag. 0 in the first Nack sent for a given sequence number, 1 in all retransmitted Nacks.
	LARQ_NACK	3 bits	NACK Count If 0 in a LARQ Control Frame, then this is a Reminder.
	LARQ_Ctl	1 bit	Set to 1 for LARQ Control Header data format
	Priority	3 bits	Link Layer Priority of this frame
Flags1_Seq0	Reserved	4 bits	Reserved, shall be 0
	LARQ_seq_high	4 bits	High 4 bits of Sequence number
Seq1	LARQ_seq_low	8 bits	Low 8 bits of Sequence number

FIG. 52e

:ontrol frame	A frame generated by a LARQ protocol module that contains only a LARQ protocol header as its payload.
Current sequence number	The most recently received new sequence number for a channel.
Data frame	Any standard Ethernet frame from higher (than LARQ) protocol layers. A LARQ-enabled station encapsulates the original payload of an Ethernet frame by inserting a LARQ header (short form control header with LARQ_hdr data) between the source address and the remainder of the frame before the frame is passed down to the driver for transmission on the network.
Forget timer	An implementation dependent mechanism to allow a receiver to reset the sequence number space of a channel when a received sequence number is not the next expected (**Current Sequence Number** + 1). One second is a suggested default value.
hold timer, lost timer	An implementation dependent timing mechanism that limits the time a receiver will hold onto a received frame while waiting for a missing frame to be retransmitted. Conceptually, there is one such timer per missing sequence number. The timer interval is **Maximum Hold Interval**.
logical channel, channel	A flow of frames from a sender to one or more receivers on a single network segment consisting of all the frames with a single combination of destination address, source address, and link layer priority.
NACK, Nack, nack	An indication from a receiver to a sender requesting retransmission of one or more frames. Also, the action of providing such an indication. E.g. "to nack a sequence number" meaning to send a NACK indication.
NACK timer	An implementation dependent timing mechanism used by a receiver to retransmit NACKs for missing sequence numbers. Conceptually, there is one such timer per missing sequence number per **logical channel**. The timer is reset each time a NACK is sent for a sequence number. The timer interval is **NACK Retransmission Interval**.
new	A new sequence number is one whose difference from the **current sequence number** for the channel, modulo the size of the sequence number space and considered as a signed integer, is greater than 0. In particular, the numbers (current + 1) through (current + 2047).
old	An old sequence number is one whose difference from the **current sequence number** for the channel, modulo the size of the sequence number space and considered as a signed integer, is less than or equal to 0. In particular, the numbers (current - 2048) through (current) are old. Note, however, that most of the old sequence numbers are also out-of-sequence.

FIG. 52f.1

out of sequence	Any sequence number that falls outside a reasonable range, old or new, of the current sequence number for a logical channel is considered out of sequence. It is recommended that plus or minus twice the value of MaximumSaveLimit (defined below) be used as the "reasonable range" when checking for out of sequence.
receiver	A station that receives frames sent on a particular channel. If the destination address is a unicast address there is at most one receiver. If the destination address is a group address (including broadcast), then there may be many receivers.
reminder	A control frame sent by the channel **sender** with the most recently used sequence number for a channel which has been inactive for **Reminder Interval** after its most recent data frame.
reminder timer	An implementation dependent timing mechanism used by a sender to generate a reminder frame after a period of inactivity for a channel. The timer is reset each time a new data frame is transmitted. Conceptually, there is one such timer per channel. The timer interval is **Reminder Interval**.
save timer	An implementation dependent timing mechanism that limits the time a sender will save a frame waiting for retransmission requests. The timer interval is **Maximum Save Interval**.
sender	The sending station for a channel, usually the station owning the source MAC address.
sequence numbers	Sequence numbers are maintained separately for each logical channel by the sender.

FIG. 52f.2

Send Sequence Number	The sequence number of the most recently transmitted data frame.
Reminder Timer Interval	A fixed interval. The default is 50 ms. Lower values will increase the overhead of reminders on network load, while higher values increase the latency for end-of-sequence frames requiring retransmission. Implementations should not use values outside of the range 25-75 ms, based on 150 ms maximum save and hold times.
Minimum Retransmission Interval	An interval used to prevent too-frequent retransmissions of a single frame. Most important for multicast channels. The default is 10 ms.
Maximum Save Limit	The maximum number of frames that will be saved for a single logical channel. This is implementation dependent, and varies with the maximum frame rate the sender is expected to support. Values of 100 or more can be useful for high-speed applications such as video.
Maximum Save Interval	The maximum time that the sender will normally save a frame for possible retransmission. The default is 150 ms.

FIG. 53

Current Sequence Number	The most recent sequence number received in a LARQ header for the channel, whether in a data frame or a reminder control frame.
Oldest missing sequence number	The oldest sequence number for a frame not yet received which has not been declared lost.
Maximum Hold Interval	The longest interval that a frame will be held awaiting an earlier missing frame. The default is to use the same value as **Maximum Save Interval**, which has a default of 150 ms
Maximum Receive Limit	The maximum number of frames that a receiver will buffer while awaiting an earlier missing frame. The default should normally be the same as the **Maximum Save Limit**.
NACK Retransmission Interval	The interval after which a receiver will retransmit a Nack control frame for a missing sequence number, with the expectation that earlier Nack control frames or data frame retransmissions were lost. The default for fixed implementations is 20 ms.

FIG54

Field	Length	Meaning
DA	6 octets	Destination Address
SA	6 octets	Source Address
Ethertype	2 octet	0x886c (Link Control Frame)
SSType	1 octet	=5
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field and ending with the second(last) octet of the Next Ethertype field. SSLength shall be >= 6 for SSVersion 0.
SSVersion	1 octet	=0
Vendor OUI	3 octets	An IEEE assigned Organizationally Unique Identifier
Control data	0-249 octets	Vendor specific control data
Next Ethertype	2 octets	= next Ethertype if an encapsulation format, or 0 if no encapsulated frame
Pad	0-38 octets	Any value octet
FCS	4 octets	

FIG. 55a

Field	Length	Meaning
DA	6 octets	Destination Address
SA	6 octets	Source Address
Ethertype	2 octet	0x886c (Link Control Frame)
LSType	2 octets	= 32769
LSLength	2 octets	Number of additional octets starting with the LSVersion field and ending with the second(last) octet of the Next Ethertype field. LSLength shall be > 6 for LSVersion 0.
LSVersion	1 octet	=0
Vendor OUI	3 octets	An IEEE assigned Organizationally Unique Identifier
Control data	1-65531 octets	Vendor specific data
Next Ethertype	2 octets	= next Ethertype if an encapsulation format, or 0 if no encapsulated frame
Pad	40-0 octets	If needed to make minimum size frame. Should be zero
FCS	4 octets	

FIG55b

carrier sense state	Output events
init	energy <= 0. Only start-of-preamble events checked.
idle	Only start-of-preamble events checked.
busy	Only end-of-preamble events checked.
transmit	Only start-of-preamble events checked (collision detection).

FIG. 56

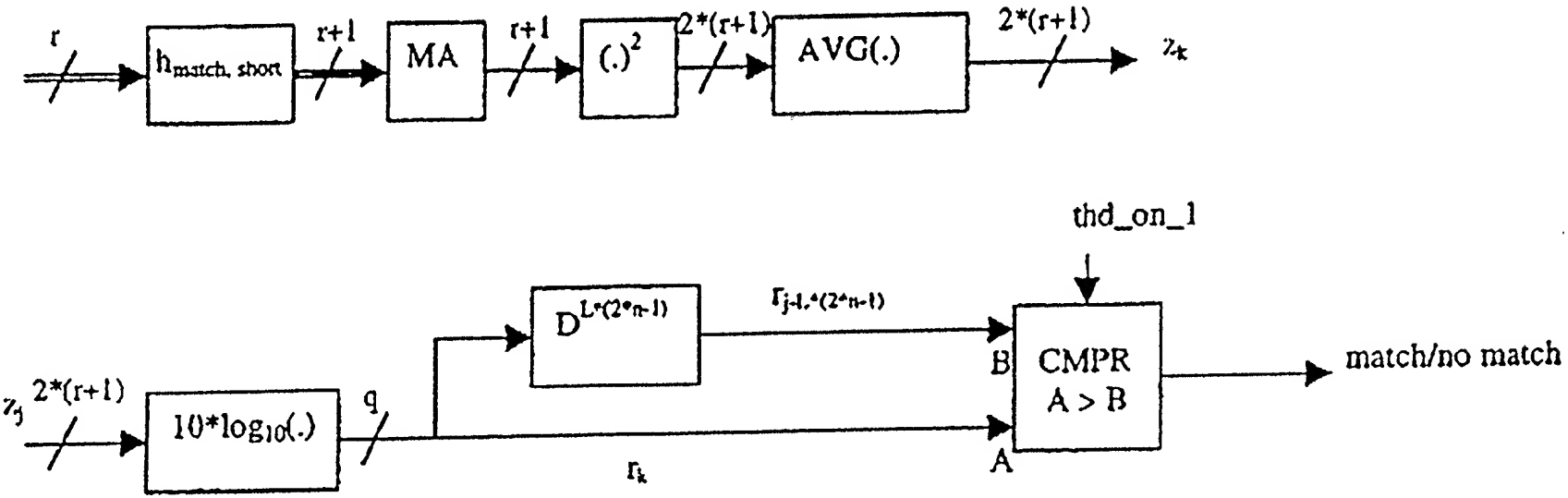


FIG. 57

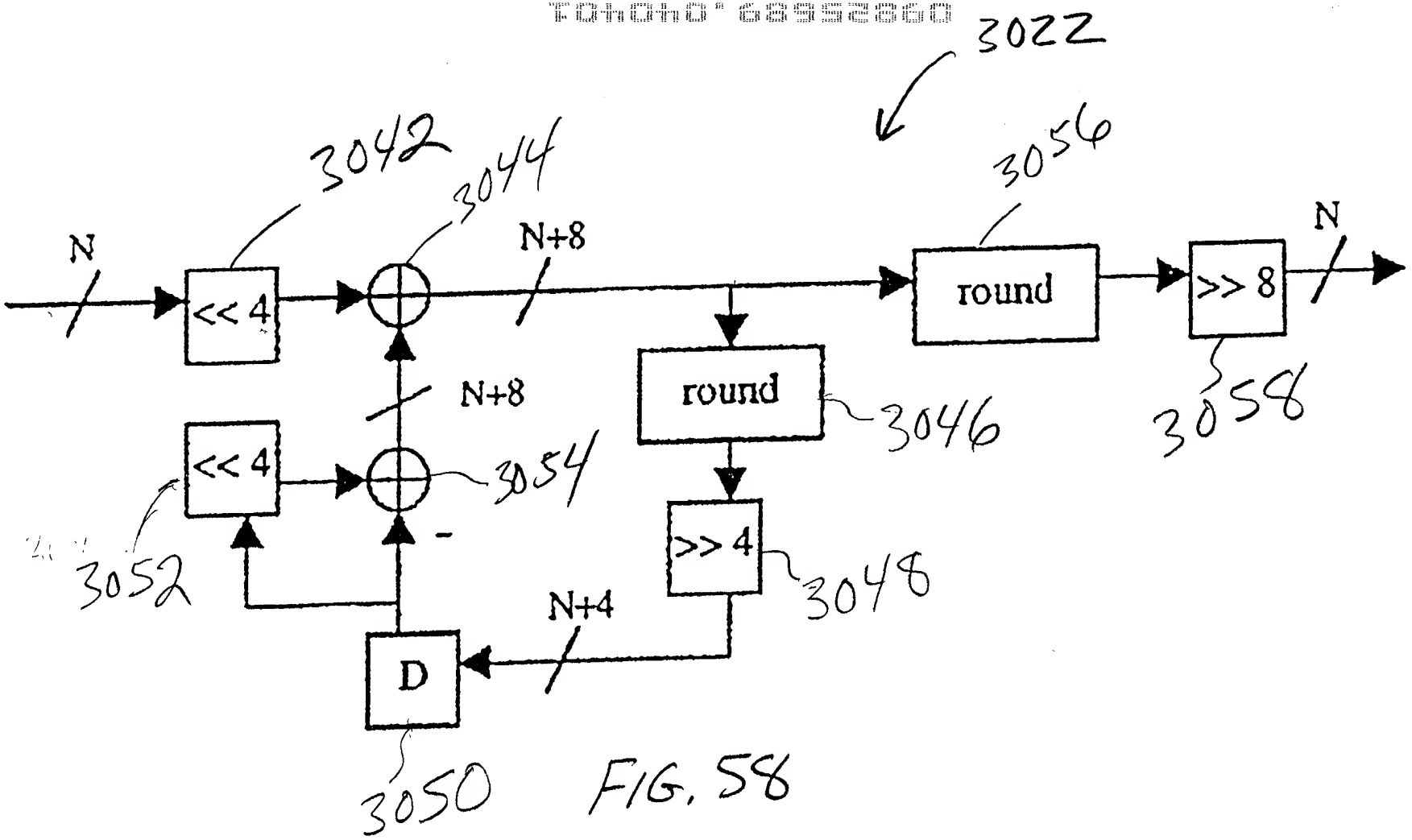

3022
3042
3044
3056
N
N+8
round
>> 8
N
<< 4
N+8
round
3046
3058
<< 4
3054
3052
-
>> 4
3048
N+4
D
3050

FIG. 58

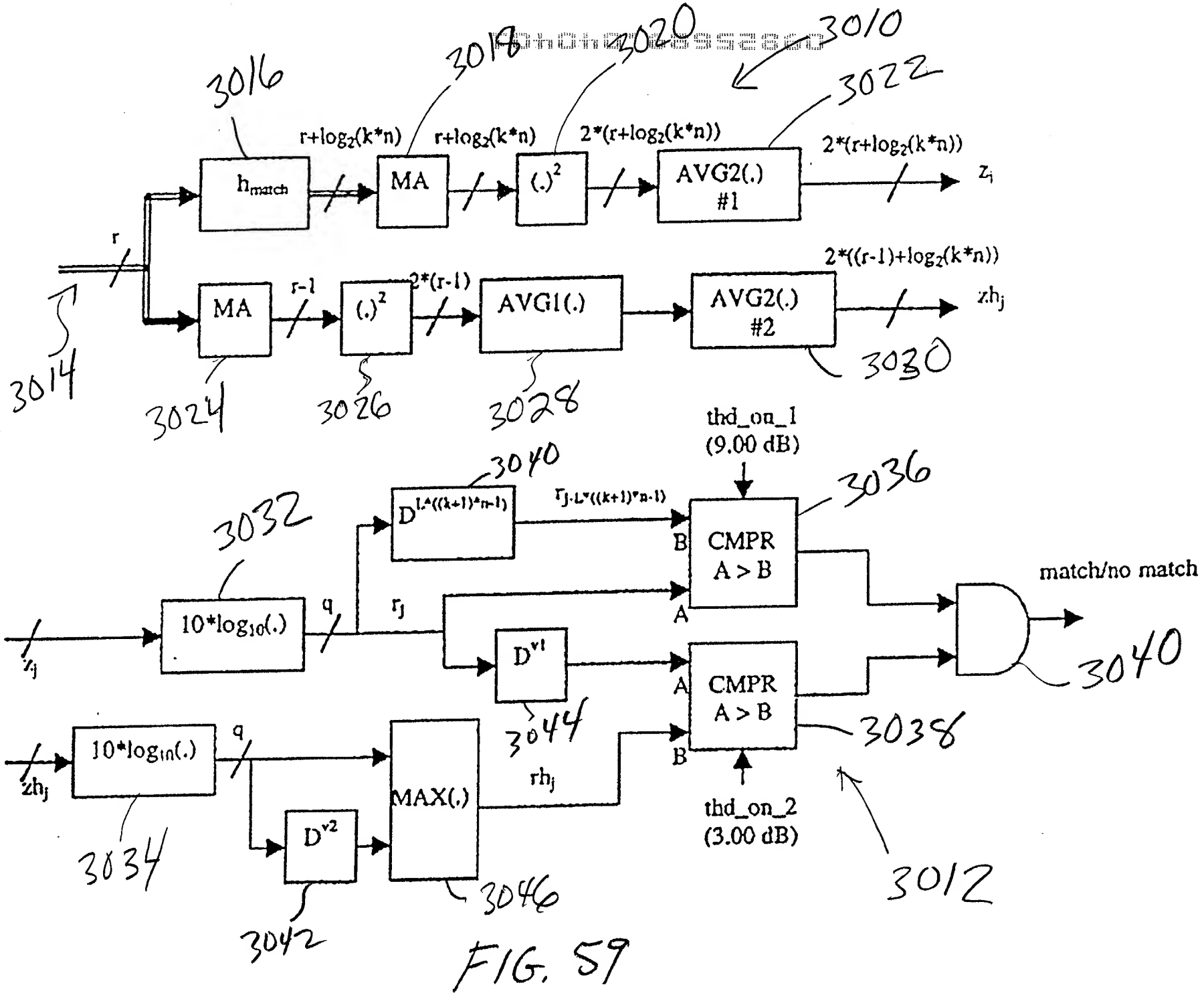

3010
3012
3014
3016
3018
3020
3022
3024
3026
3028
3030
3032
3034
3036
3038
3040
3042
3044
3046
h_{match}
MA
$(.)^2$
AVG2(.) #1
AVG1(.)
AVG2(.) #2
$r+\log_2(k*n)$
$2*(r+\log_2(k*n))$
$2*((r-1)+\log_2(k*n))$
r
r-1
$2*(r-1)$
z_i
zh_j
$10*\log_{10}(.)$
q
r_j
$D^{L*((k+1)*n-1)}$
$r_j \cdot L^{*((k+1)*n-1)}$
D^{v1}
D^{v2}
MAX(.)
rh_j
CMPR A > B
A
B
thd_on_1 (9.00 dB)
thd_on_2 (3.00 dB)
match/no match

FIG. 59

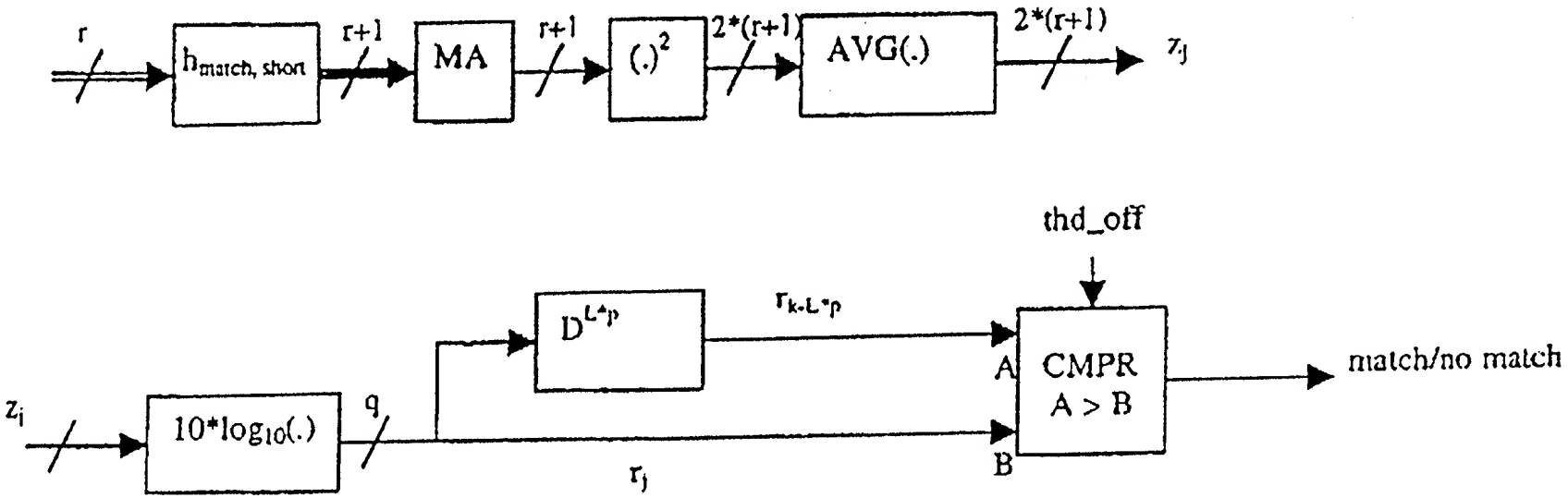

r
h match, short
r+1
MA
r+1
(.)2
2*(r+1)
AVG(.)
2*(r+1)
zj
thd_off
D L*p
rk-L*p
A
CMPR
A > B
match/no match
zi
10*log10(.)
q
rj
B

FIG. 60

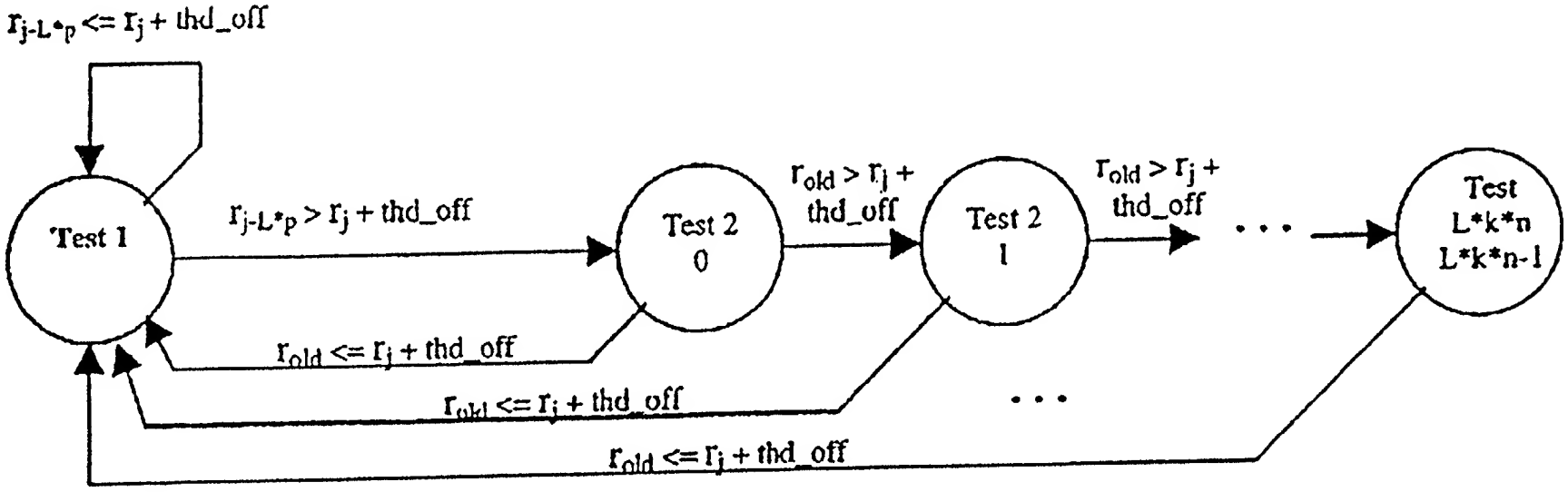

rj-L*p <= rj + thd_off
Test 1
rj-L*p > rj + thd_off
Test 2
0
rold > rj + thd_off
Test 2
1
rold > rj + thd_off
Test
L*k*n
L*k*n-1
rold <= rj + thd_off
rold <= rj + thd_off
rold <= rj + thd_off

FIG. 61

Table Index	Table Value (dB)
0	0.00
1	3.00
2	6.00
3	9.00
4	12.00
5	15.00
6	18.00
7	21.00
8	24.00
9	27.00
10	30.00
11	33.00
12	36.00
13	39.25
14	42.25
15	45.25
16	48.25
17	51.25
18	54.25
19	57.25
20	60.25
21	63.25
22	66.25
23	69.25
24	72.25
25	75.25
26	78.25
27	81.25
28	84.25
29	87.25
30	90.25
31	93.25

FIG. 62a

Table Index	Table Value (dB)
0	0.00
1	0.25
2	0.25
3	0.50
4	0.50
5	0.75
6	0.75
7	0.75
8	1.00
9	1.00
10	1.25
11	1.25
12	1.50
13	1.50
14	1.50
15	1.75
16	1.75
17	1.75
18	2.00
19	2.00
20	2.00
21	2.25
22	2.25
23	2.25
24	2.50
25	2.50
26	2.50
27	2.75
28	2.75
29	2.75
30	2.75
31	3.00

FIG. 626

FIG. 63a

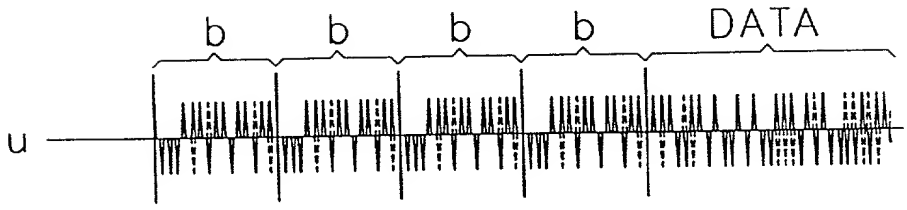
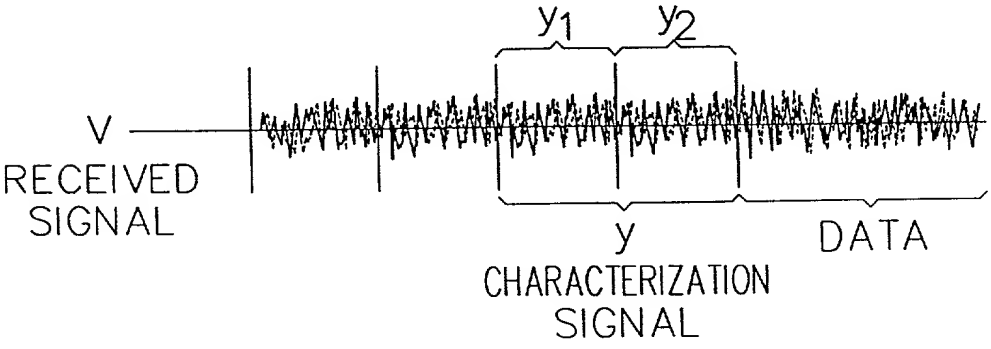


FIG. 63b

FIG. 63c



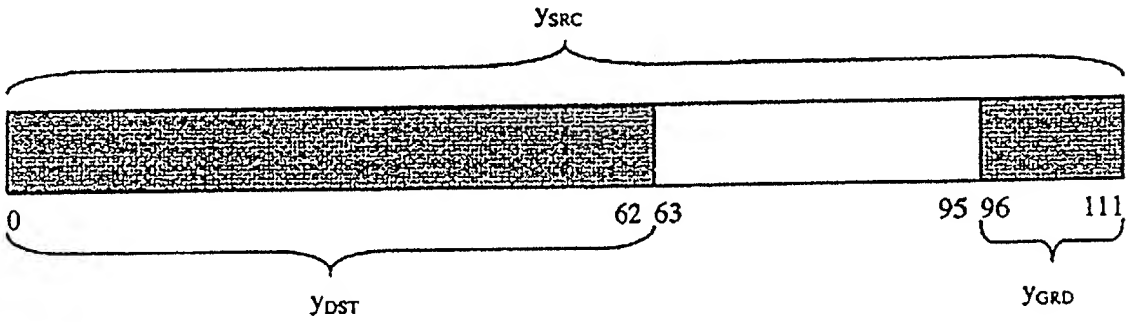

YSRC
0
62 63
95 96
111
YDST
YGRD

FIG. 64

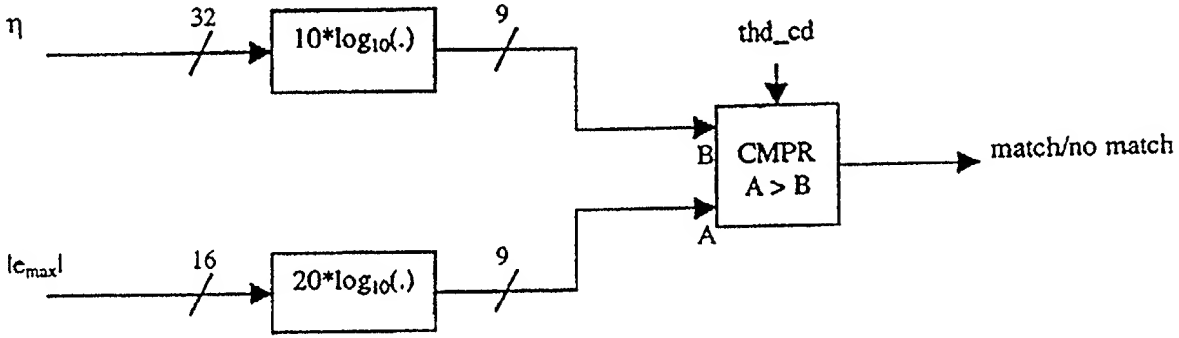

η
32
10*log10(.)
9
thd_cd
B
CMPR
A > B
match/no match
A
|emax|
16
20*log10(.)
9

FIG. 65

Table Index	Table Value
0	0.00
1	6.00
2	12.00
3	18.00
4	24.00
5	30.00
6	36.00
7	42.25
8	48.25
9	54.25
10	60.25
11	66.25
12	72.25
13	78.25
14	84.25
15	90.25

FIG. 66a

Table Index	Table Value
0	0.00
1	0.50
2	1.00
3	1.50
4	2.00
5	2.25
6	2.75
7	3.25
8	3.50
9	4.00
10	4.25
11	4.50
12	4.75
13	5.25
14	5.50
15	5.75

FIG. 66b

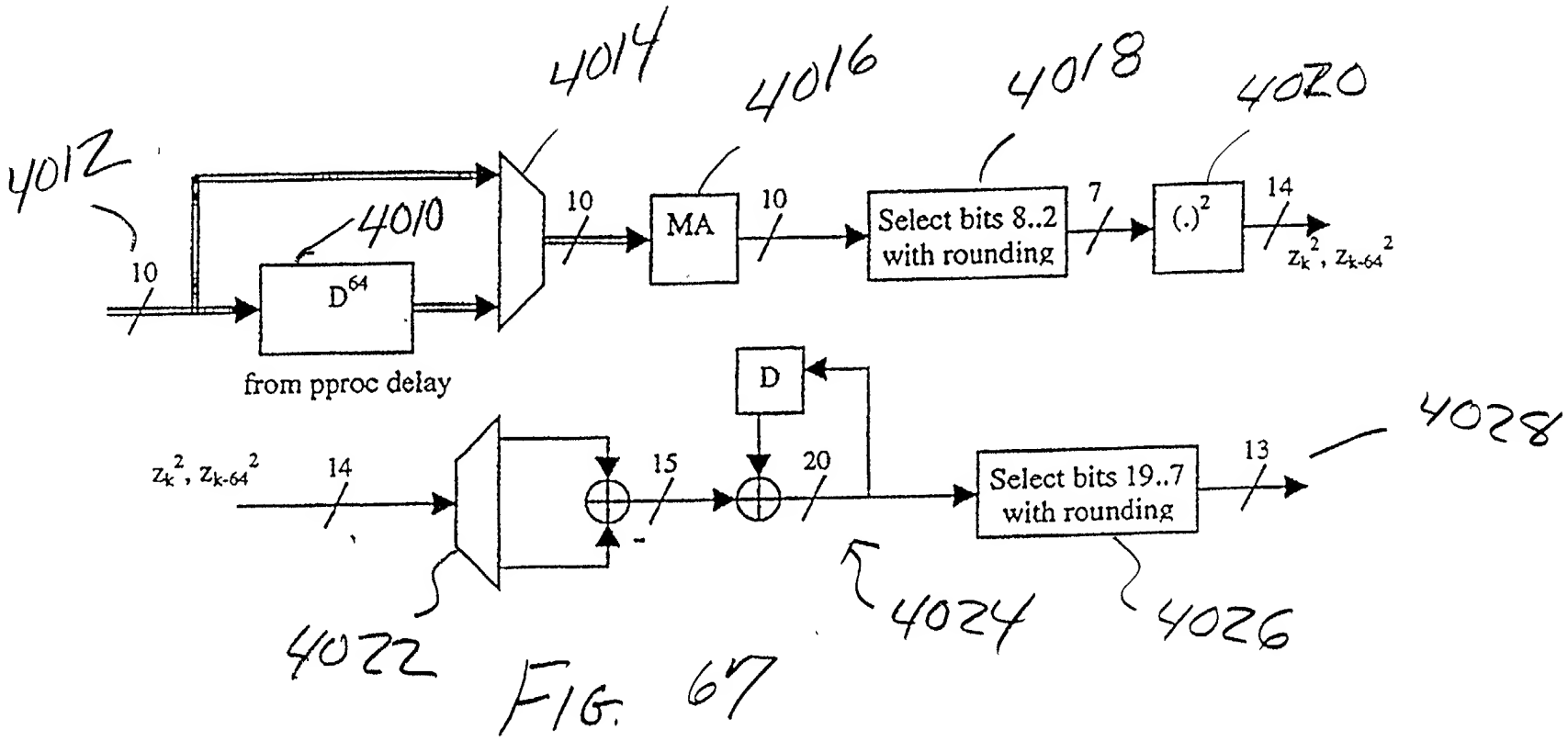

4014
4016
4018
4020
4012
4010
10
D^64
from pproc delay
10
MA
10
Select bits 8..2
with rounding
7
(.)^2
14
z_k^2, z_k-64^2
D
z_k^2, z_k-64^2
14
15
20
Select bits 19..7
with rounding
13
4028
4022
4024
4026

FIG. 67

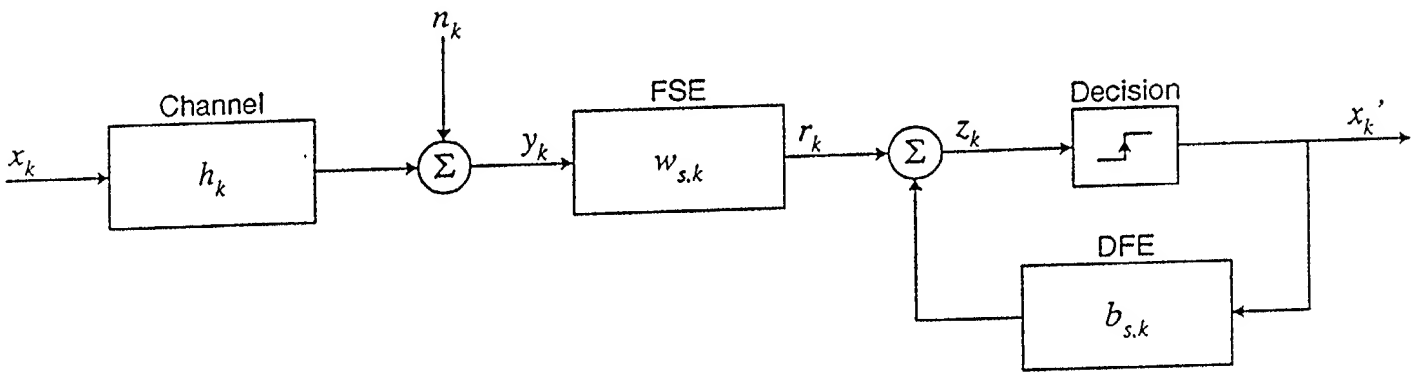

n_k
Channel
x_k
h_k
Σ
y_k
FSE
$w_{s,k}$
r_k
Σ
z_k
Decision
x_k'
DFE
$b_{s,k}$

FIG. 68

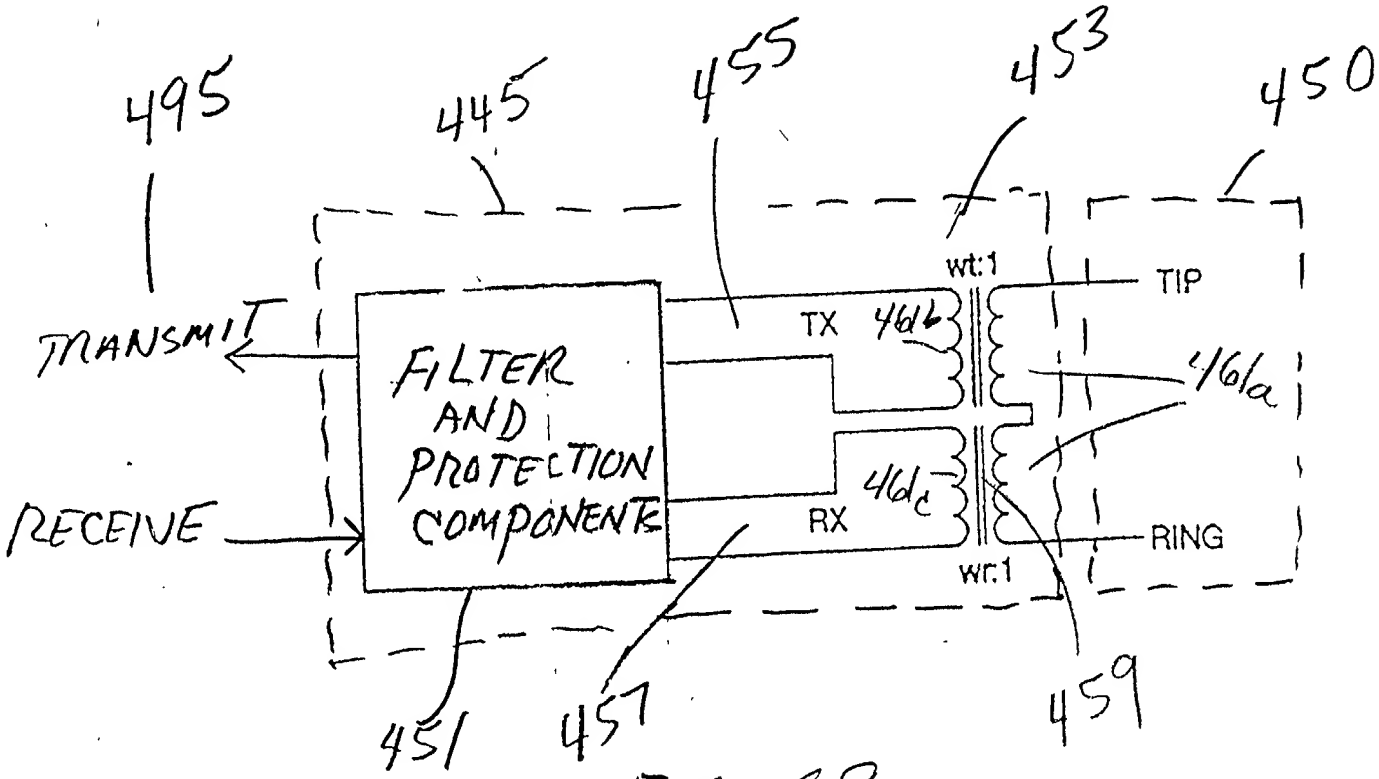


FIG. 69

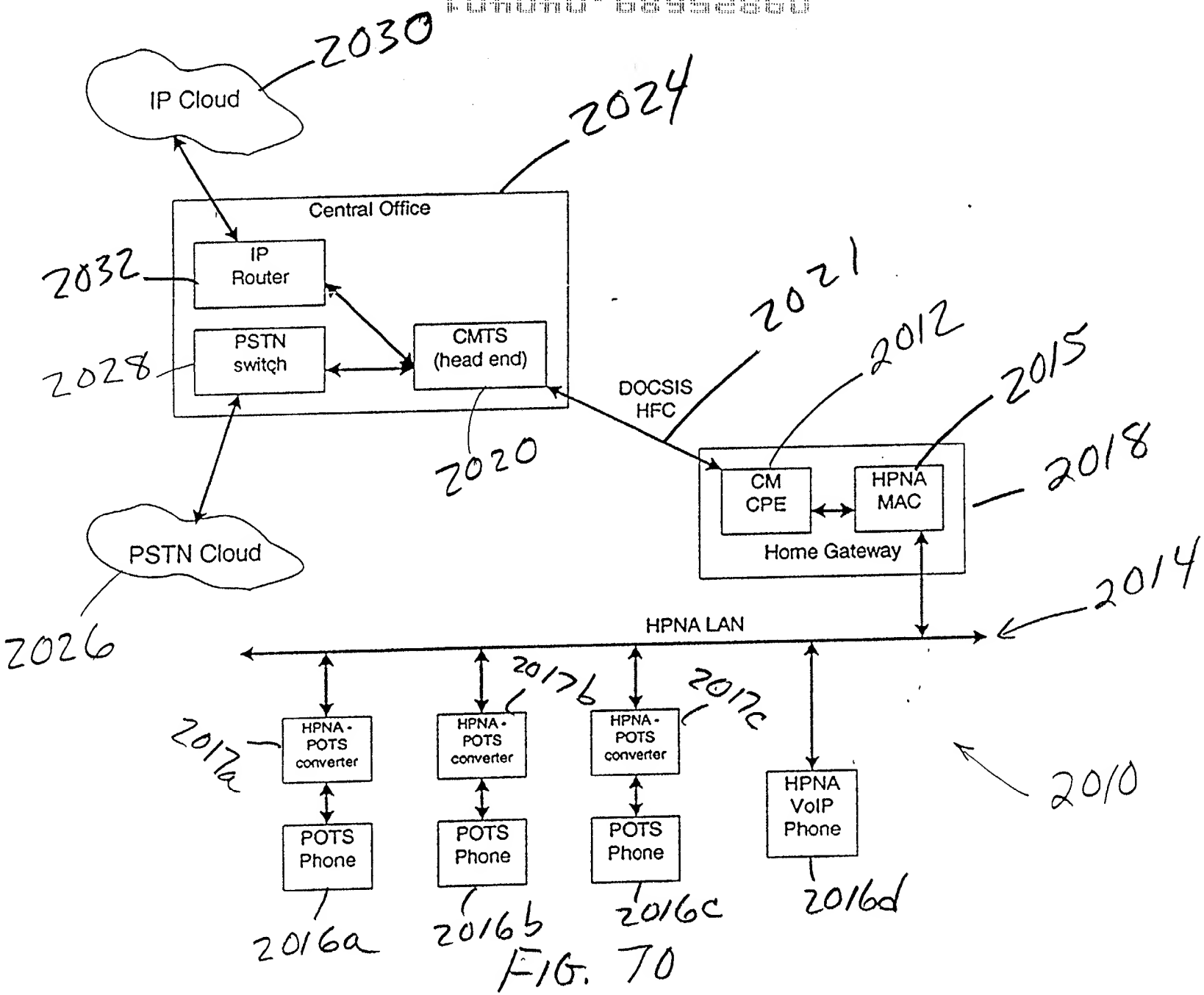


FIG. 10

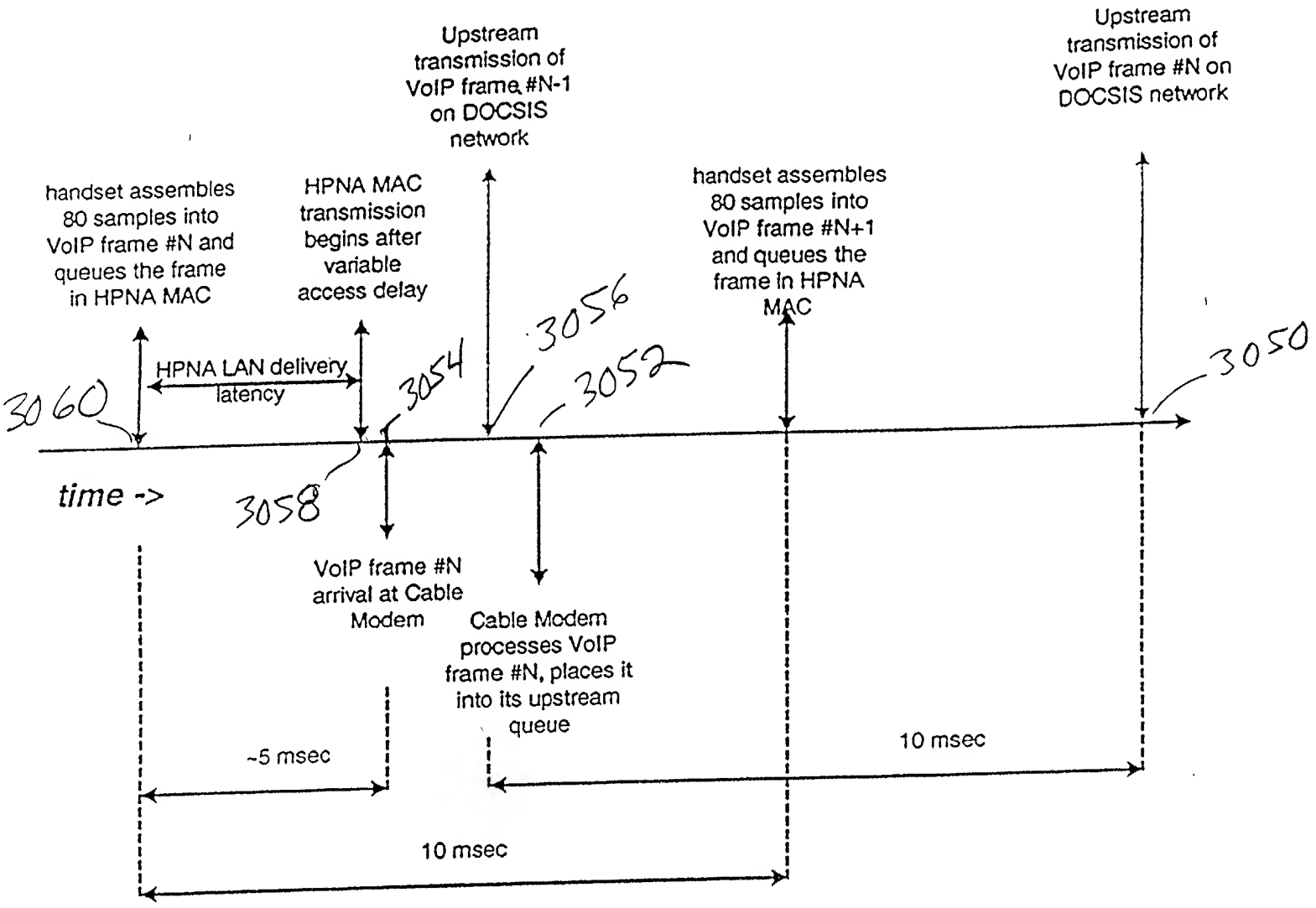

Upstream transmission of VoIP frame #N-1 on DOCSIS network
Upstream transmission of VoIP frame #N on DOCSIS network
handset assembles 80 samples into VoIP frame #N and queues the frame in HPNA MAC
HPNA MAC transmission begins after variable access delay
handset assembles 80 samples into VoIP frame #N+1 and queues the frame in HPNA MAC
HPNA LAN delivery latency
3060
3054
3056
3052
3050
3058
time ->
VoIP frame #N arrival at Cable Modem
Cable Modem processes VoIP frame #N, places it into its upstream queue
~5 msec
10 msec
10 msec

FIG. 71

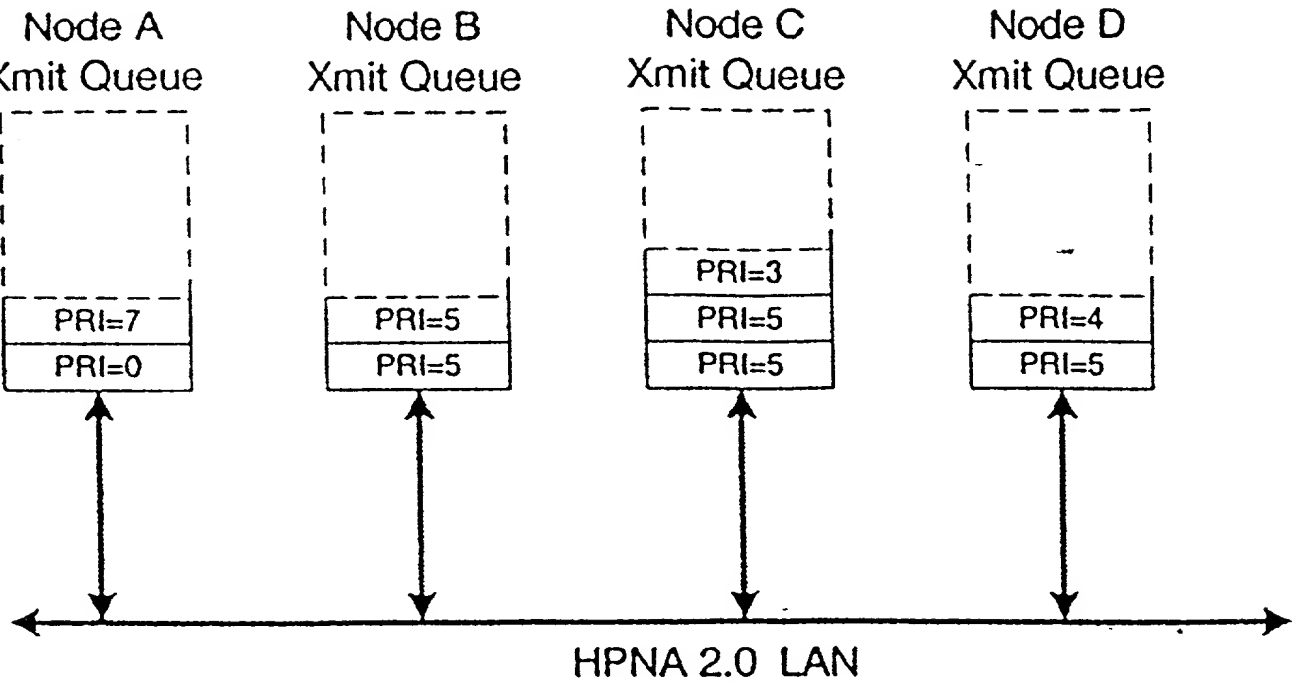


FIG. 72a

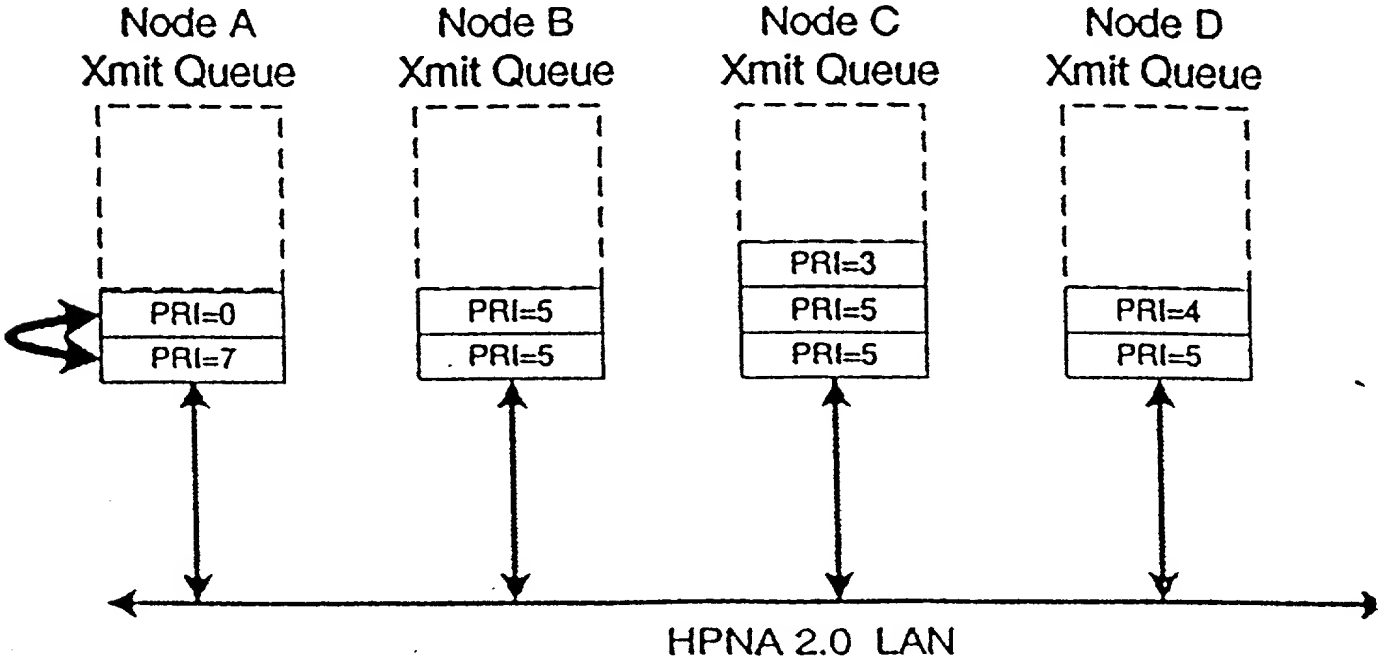


FIG. 72b

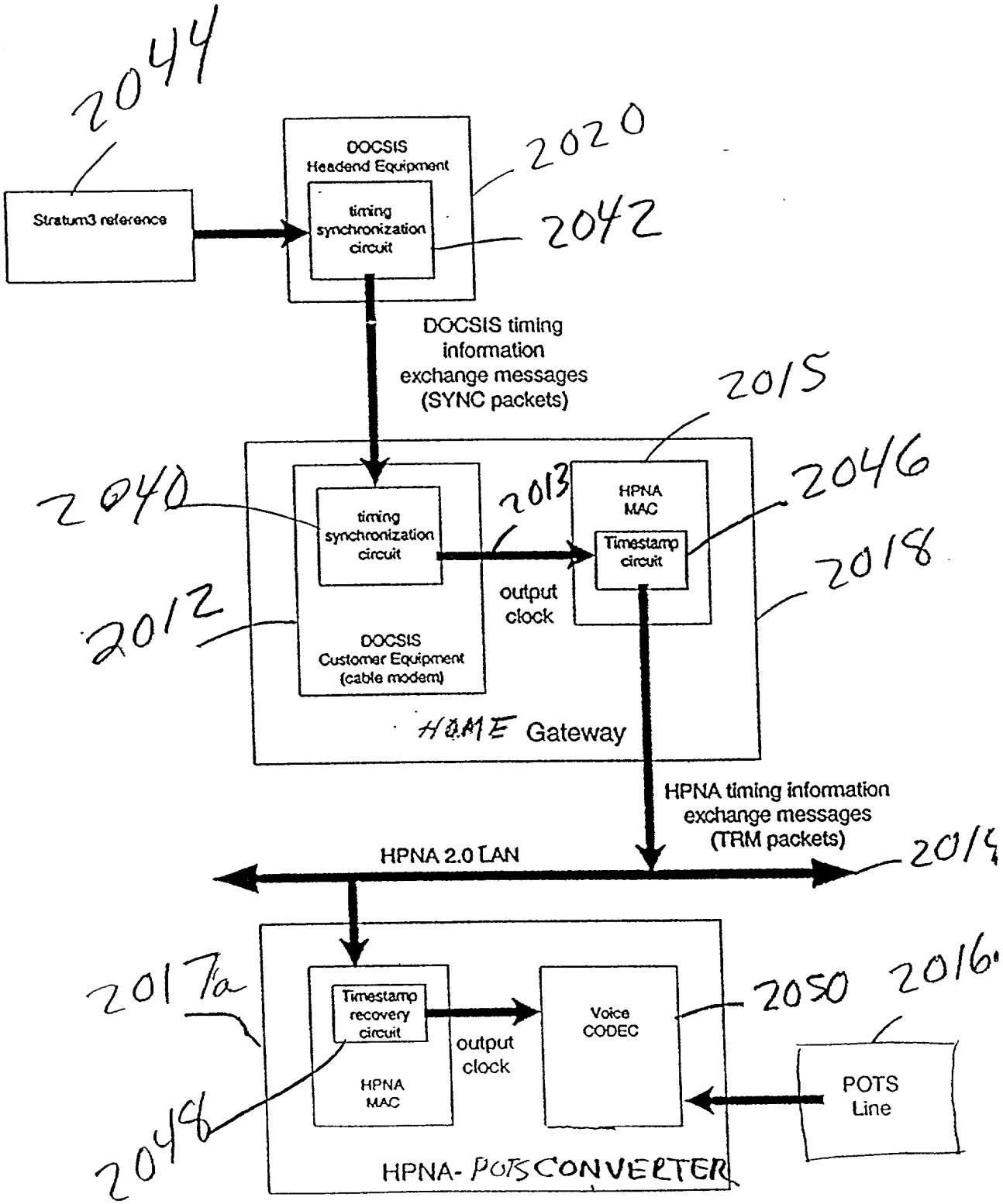

2044
Stratum3 reference
DOCSIS
Headend Equipment
2020
timing
synchronization
circuit
2042
DOCSIS timing
information
exchange messages
(SYNC packets)
2015
2040
timing
synchronization
circuit
2013
HPNA
MAC
2046
Timestamp
circuit
2018
output
clock
2012
DOCSIS
Customer Equipment
(cable modem)
HOME Gateway
HPNA timing information
exchange messages
(TRM packets)
HPNA 2.0 LAN
2014
2017a
Timestamp
recovery
circuit
output
clock
Voice
CODEC
2050
2016
POTS
Line
2048
HPNA
MAC
HPNA-POTS CONVERTER

FIG. 73

parameter	UPSTREAM "10E-6 Case	91% Case	90% Case	DOWNSTREAM "10E-6 Case	91% Case	90% Case
Access delay	3.1	1.3	1.3	3.1	1.3	1.3
Collision Resolution	2.7	2.7	0.8	2.7	2.7	0.8
3 up, 1 down	2.1	1.0	1.0	2.1	1.0	1.0
last up	0.5	0.3	0.3	0.5	0.3	0.3
Collision Resolution	0.8	0.8	0.8	0.8	0.8	0.8
3 up, 1 down	2.1	1.0	1.0	2.1	1.0	1.0
last up	0.5	0.3	0.3	0.5	0.3	0.3
3 down				1.5	0.8	0.8
3 down				1.5	0.8	0.8
Total latency	11.8	7.4	5.5	14.9	8.9	7.1

10E-6 case is 10E-6 CRA once of two tries in homes with maximum 4Mbits/sec raw rate
91% case is 10E-6 CRA once of two tries in homes with minimum 10Mbits/sec raw rate
90% case is 10E-1 CRA twice in two tries in homes with minimum 10Mbits/sec raw rate

Values in the table above are in milliseconds.

Overheads:

					linear PCM	5 nodes	5 nodes	5 nodes
ifg	per coll	frame hdr	Larq hdr	rtp_hdr	frame size	CRA 10E-6	CRA 10E-1	CRA fixed
0.018	0.206	0.07	8	40	160	13	4	2
msec	msec	msec	Bytes	bytes	bytes	collisions	collisions	collisions

Frame header includes preamble, FC, DA, SA, T/L, EOF

FIG. 74

parameter	*UPSTREAM* "10E-6 Case	91% Case	90% Case	*DOWNSTREAM* "10E-6 Case	91% Case	90% Case
Access delay	3.1	1.3	1.3	3.1	1.3	1.3
Collision Resolution	0.4	0.4	0.4	0.4	0.4	0.4
3 up, 1 down	1.4	0.8	0.8	1.4	0.8	0.8
last up	0.5	0.3	0.3	0.5	0.3	0.3
Collision Resolution	0.0	0.0	0.0	0.0	0.0	0.0
3 up, 1 down	0.0	0.0	0.0	0.0	0.0	0.0
last up	0.0	0.0	0.0	0.0	0.0	0.0
3 down				1.1	0.6	0.6
3 down				0.0	0.0	0.0
Total latency	5.5	2.7	2.7	6.5	3.3	3.3

FIG. 75

Field	Length	Meaning
DA	6 octets	Destination Address
SA	6 octets	Source Address
Ethertype	2 octets	(TBD) = VOHN Link Control Frame - new IEEE assignment
Type	2 octets	1 = Timestamp Sync Message
Length	2 octets	= 4
Version	2 octets	= 0
SeqNum	2 octets	Timestamp Sync Message Sequence Number
Pad		Any value octet
FCS	4 octets	Frame Check Sequence

FIG. 76

Field	Length	Meaning
DA	6 octets	Destination Address
SA	6 octets	Source Address
Ethertype	2 octets	(TBD) = VOHN Link Control Frame - new IEEE assignment
Type	2 octets	2 = Timestamp Report Message
Length	2 octets	Number of additional octets in the signaling frame, starting with Version field and ending with the last octet of the Data Payload field. Minimum is 2.
Version	2 octets	= 0
TSMSeqNum	2 octets	Sequence number of TSM to which the Timestamp in this message is applicable.
Timestamp	4 octets	Timestamp of a previously transmitted Timestamp Report Message, corresponding to TSMSeqNum.
Frequency	2 octets	Resolution of the timestamp and Gtimestamp fields, in ticks/1.000ms. For example, value 32768 corresponds to one clock tick at 32.768Mhz, in which the LSBit of the Timestamp corresponds to a time of 0.030517578125usec. The Timestamp will rollover every 131 seconds = 2.2 minutes
NumGrants	2 octets	Number of Grant Timestamps specified in the payload of this control message. NumGrants may be zero. Each grant timestamp is accompanied by a Line ID and Call ID field. Including the Grant Timestamp, the total for each grant timestamp is 8 bytes.

FIG. 77(1)

Line ID	2 octets	Identifier of the Line termination associated with the immediately following GTimestamp.
Call ID	2 octets	Identifier of the call instance on the Line termination associated with the immediately following GTimestamp.
GrantTimestamp	4 octets	Grant Timestamp corresponding to the immediately preceding Line ID. This is the time at which the Proxy Gateway wishes to receive a future constant bit rate service flow packet in order to minimize delivery latency to subsequent delivery to a synchronous network. The time value corresponds to the time at the timing master. Additional packets for the identified service flow are expected to arrive at periodic intervals measured from this time.
...		additional instances of {Line ID, Call ID, Grant Timestamp} field tuples
Pad		Any value octet
FCS	4 octets	Frame Check Sequence

FIG. 77(2)

PIN NAME	CM-side Function (HPNA timing master)		Handset Function (HPNA timing slave)	
DPLL_REF_CLK	DPLL input clock	IN		
Grant[4]	Grant Present Indication	IN		
Grant[3]	Grant SID Value[3]	IN		
Grant[2]	Grant SID Value[2]	IN		
Grant[1]	Grant SID Value[1]	IN		
Grant[0]	Grant SID Value[0]	IN		
V_CLK_OUT			DPLL output clock	OUT
GPI[0]			Grant Present Indication[0]	OUT
GPI[1]			Grant Present Indication[1]	OUT

FIG. 78

PIN NAME	CM-side Function (HPNA timing master)		Handset Function (HPNA timing slave)	
DPLL_REF_CLK	DPLL input clock	IN		
Grant[4]	Grant Present Indication	IN		
Grant[3]	Grant SID Value[3]	IN		
Grant[2]	Grant SID Value[2]	IN		
Grant[1]	Grant SID Value[1]	IN		
Grant[0]	Grant SID Value[0]	IN		
V_CLK_OUT			DPLL output clock	OUT
Frame[0]			Frame boundary marker[0]	OUT
Frame[1]			Frame boundary marker[1]	OUT

FIG. 79

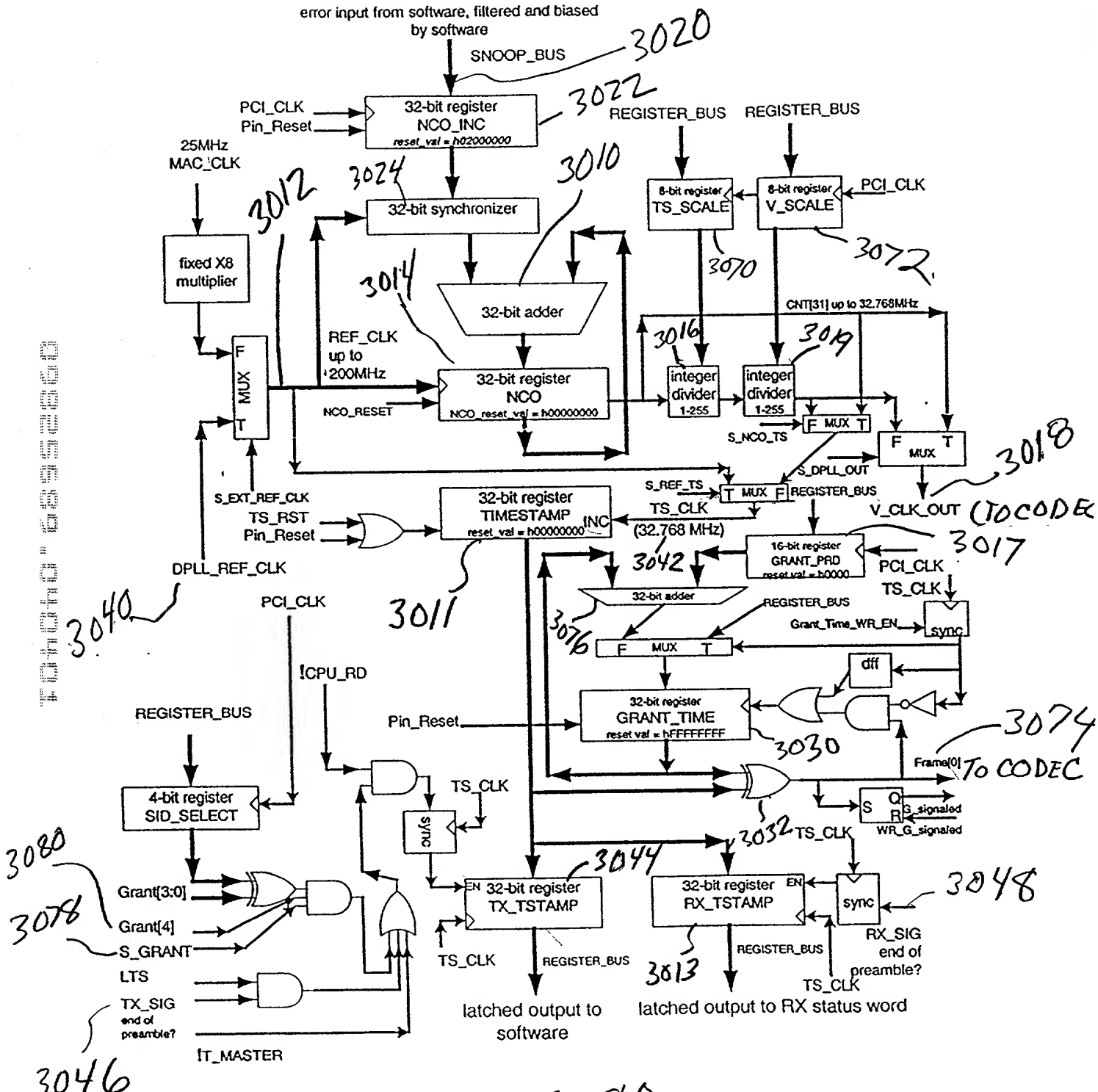

error input from software, filtered and biased by software
SNOOP_BUS
3020
PCI_CLK
Pin_Reset
32-bit register NCO_INC
reset_val = h02000000
3022
REGISTER_BUS
REGISTER_BUS
25MHz MAC_CLK
3012
3024
32-bit synchronizer
3010
8-bit register TS_SCALE
8-bit register V_SCALE
PCI_CLK
3070
3072
fixed X8 multiplier
3014
32-bit adder
CNT[31] up to 32.768MHz
3016
3019
REF_CLK up to 200MHz
F MUX T
32-bit register NCO
NCO_reset_val = h00000000
NCO_RESET
integer divider 1-255
integer divider 1-255
F MUX T
S_NCO_TS
F MUX T
3018
S_DPLL_OUT
V_CLK_OUT
(TO CODEC
S_EXT_REF_CLK
TS_RST
Pin_Reset
32-bit register TIMESTAMP
reset_val = h00000000
INC
S_REF_TS
T MUX F
REGISTER_BUS
TS_CLK
(32.768 MHz)
3017
16-bit register GRANT_PRD
reset_val = h0000
PCI_CLK
TS_CLK
DPLL_REF_CLK
3040
PCI_CLK
3011
3042
32-bit adder
REGISTER_BUS
Grant_Time_WR_EN
sync
3076
F MUX T
dff
!CPU_RD
REGISTER_BUS
Pin_Reset
32-bit register GRANT_TIME
reset val = hFFFFFFFF
3030
3074
Frame[0]
To CODEC
TS_CLK
4-bit register SID_SELECT
sync
S Q R
G_signaled
WR_G_signaled
3032
TS_CLK
3080
3044
3048
Grant[3:0]
Grant[4]
3078
S_GRANT
LTS
TX_SIG end of preamble?
3046
!T_MASTER
EN 32-bit register TX_TSTAMP
EN 32-bit register RX_TSTAMP
sync
RX_SIG end of preamble?
TS_CLK
REGISTER_BUS
TS_CLK
REGISTER_BUS
3013
TS_CLK
latched output to software
latched output to RX status word

FIG. 80

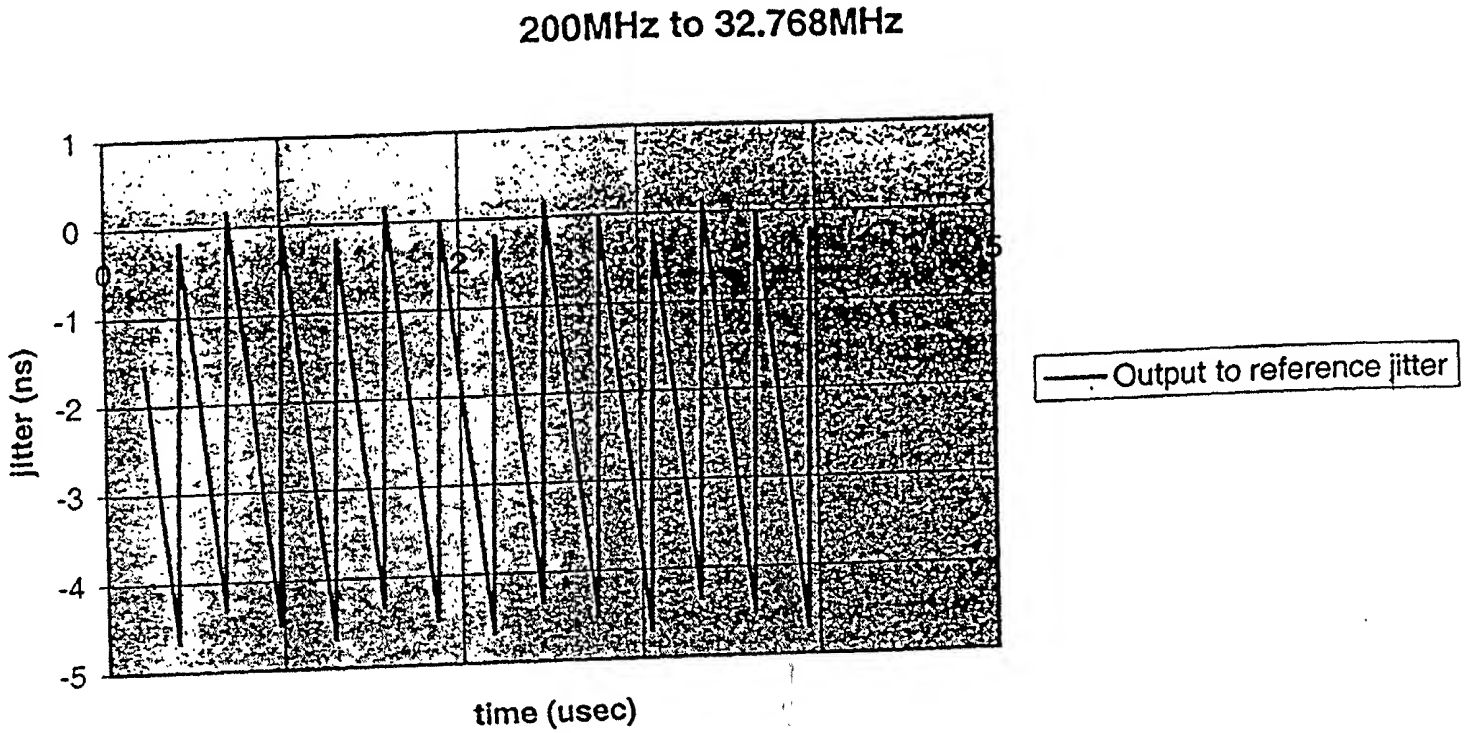


FIG. 81

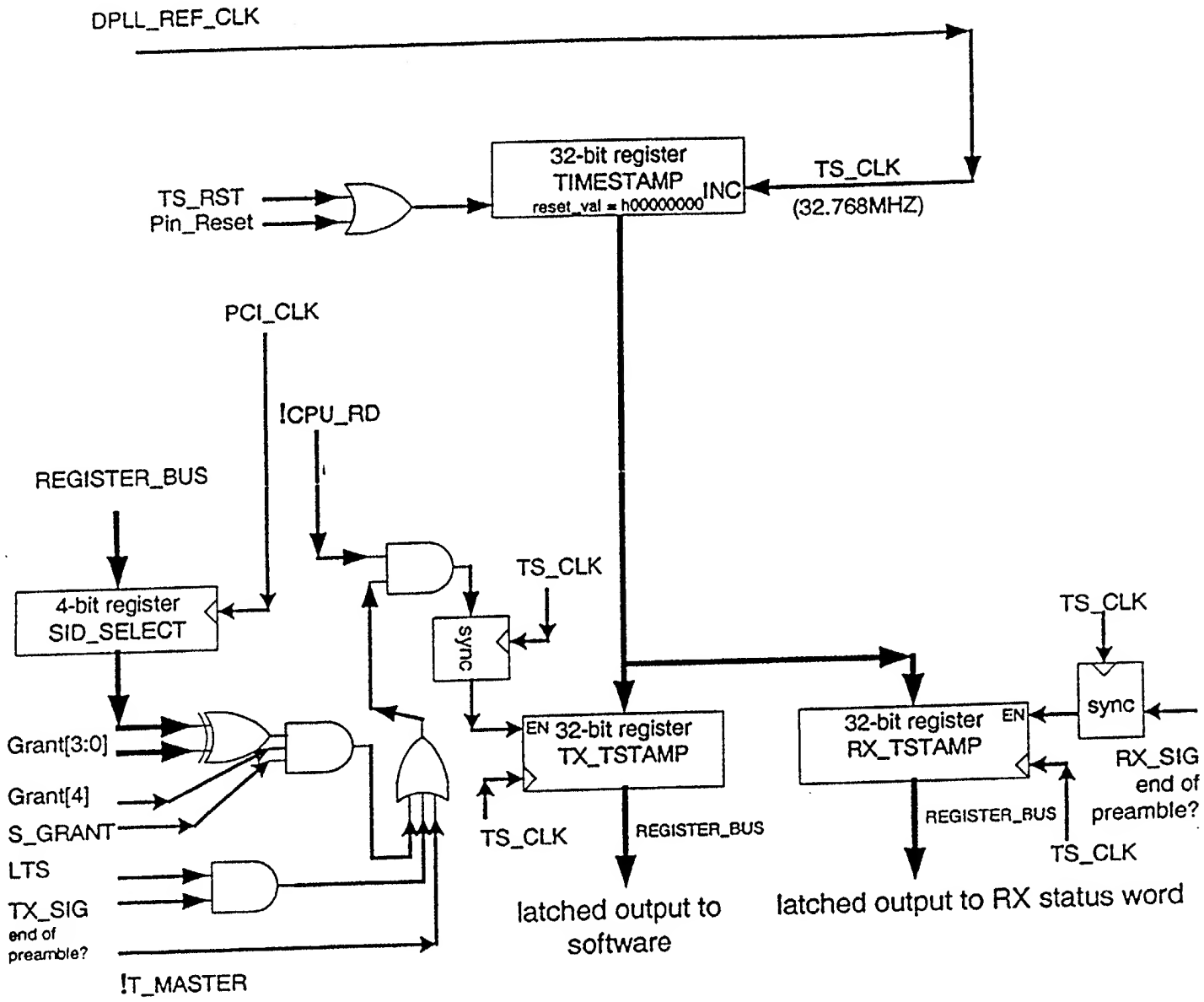

DPLL_REF_CLK
32-bit register
TIMESTAMP
reset_val = h00000000
INC
TS_CLK
(32.768MHZ)
TS_RST
Pin_Reset
PCI_CLK
!CPU_RD
REGISTER_BUS
4-bit register
SID_SELECT
TS_CLK
sync
TS_CLK
sync
EN
32-bit register
TX_TSTAMP
EN
32-bit register
RX_TSTAMP
RX_SIG
end of
preamble?
Grant[3:0]
Grant[4]
S_GRANT
LTS
TX_SIG
end of
preamble?
!T_MASTER
TS_CLK
REGISTER_BUS
REGISTER_BUS
TS_CLK
latched output to
software
latched output to RX status word

FIG. 82

PIN NAME	**CM-side Function (HPNA timing master)**		**Handset Function (HPNA timing slave)**	
DPLL_REF_CLK	Timestamp input clock	IN	Timestamp input clock	
Grant[4]	Grant Present Indication	IN	NA	
Grant[3]	Grant SID Value[3]	IN	NA	
Grant[2]	Grant SID Value[2]	IN	NA	
Grant[1]	Grant SID Value[1]	IN	NA	
Grant[0]	Grant SID Value[0]	IN	NA	

FIG. 83a

Bit locations	Field name	Description
7-3	Reserved	
2	TsReset	When set to 1, forces timestamp register to value of 0x00000000. When set to 0, allows timestamp register to increment by one for each detected DPLL_REF_CLK rising edge.
1	SGrant	When set to 1, causes timestamp to be latched into txTimeStampHigh and txTimeStampLow registers whenever the value of tscSID matches the value of input pins Grant[3:0] and Grant[4] is asserted. When set to 0, disables txTimeStampHigh and txTimeStampLow latching under the stated conditions.
0	TMaster	When set to 1, enables txTimestampHigh and txTimestampLow registers to be latched with timestamp values at times determined by frame transmissions (through the LTS descriptor bit) or grant events (through the sGrant descriptor bit). When set to 0, enables txTimestampHigh and txTimestampLow registers to be latched with timestamp values at times determined by txTimeStampHigh and txTimeStampLow register read accesses.

Default value of this register is 0x05

FIG. 83b

Bit locations	Field name	Description
7-4	Reserved	
3-0	SID	SID value that is to be matched by Grant[3:0] pins in order to cause a grant timestamp value to be latched. When the Grant[3:0] pins match the SID value and the Grant[4] input is 1 and the sGrant register bit is 1, then the current timestamp value will be latched into the txTimeStampHigh and txTimeStampLow registers.

Default value of this register is 0x00

FIG. 83c

Bit locations	Field name	Description
15-0	txTimeStampLow	Least significant 16 bits of the latched tx timestamp value

Default value of this register is undefined.

FIG. 83d

Bit locations	Field name	Description
15-0	txTimeStampHigh	Most significant 16 bits of the latched tx timestamp value

Default value of this register is undefined.

FIG. 83e

Bit locations	Field name	Description
15-0	rxTimeStampLow	Least significant 16 bits of the latched rx timestamp value

Default value of this register is undefined.

FIG. 83f

Bit locations	Field name	Description
15-0	rxTimeStampHigh	Most significant 16 bits of the latched rx timestamp value

Default value of this register is undefined.

FIG. 83g

DPLL Output Jitter
TS=24.576MHz, TRM=1.0sec, lg=0.9, ig=0.1, tgood=0.95,
m_j_dev=1ppm

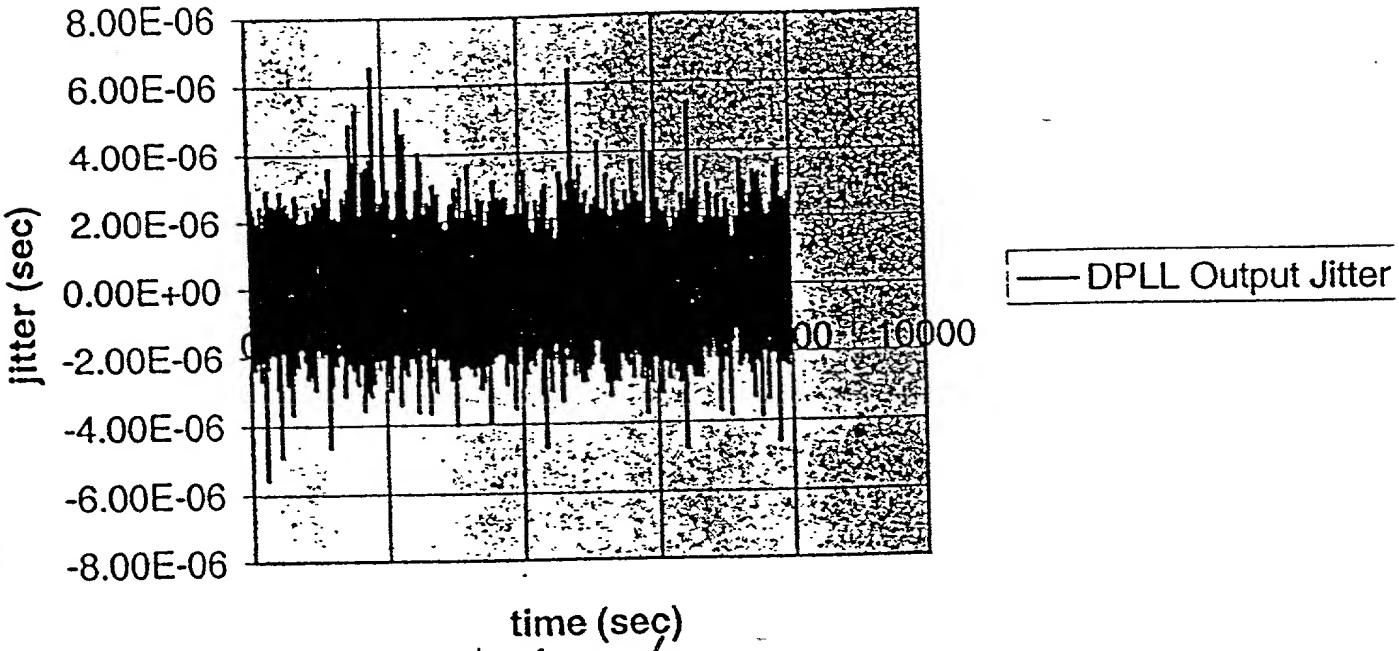


Fig. 84a

DPLL Output Jitter
TS=24.576MHz, TRM=1.0sec, lg=0.9, ig=0.1, tgood=0.95,
m_j_dev=0ppm

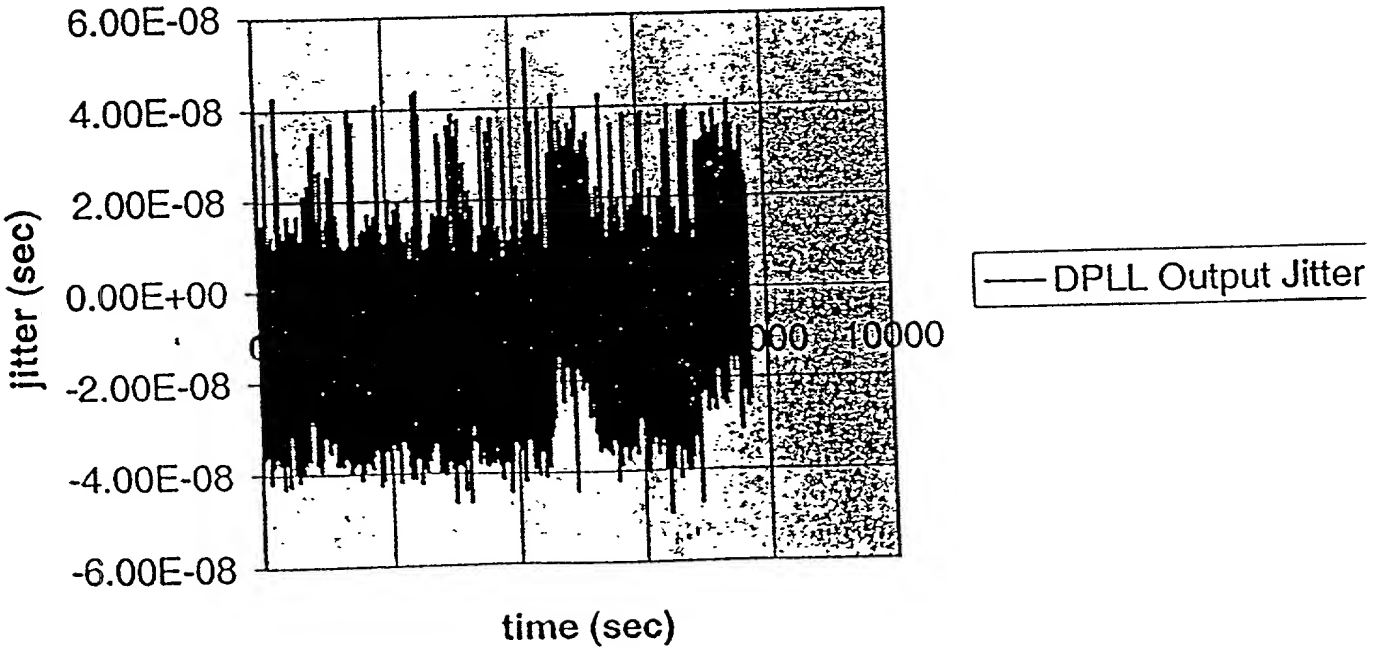


Fig 84b

Field	Length	Meaning
DA	6 octets	Destination Address (FF.FF.FF.FF.FF.FF)
SA	6 octets	Source Address
Ethertype	2 octets	0x886c (HPNA Link Control Frame)
SSType	1 octet	= TBD
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field and ending with the second (last) octet of the Next Ethertype field. Minimum is 16.
SSVersion	1 octet	= 0
TRM_type	1 octet	Value of x00 means that this is a TRM containing a valid timestamp. Value of x01 means that the master does not have a valid clock and slaves should give local indication that they are no longer locked to a master reference. Value of x80 means that this is a TQM. Value of x81 means that this is a TSM. All other values are reserved.
TRMSeqNum	2 octets	Timestamp Report Message Sequence Number for this message. Sequence number of x0000 indicates an initial TRM, implying that Timestamp and PrevTRMSeqNum are both invalid.
PrevTRMSeqNum	2 octets	Sequence number of TRM to which the Timestamp in this message is applicable. The value of PrevTRMSeqNum is *not* necessarily equal to TRMSeqNum minus one. PrevTRMSeqNum is set to x0000 for the first TRM of a TRM pair.

FIG. 8(1)

Field	Length	Meaning
Timestamp	4 octets	Timestamp of a previously transmitted Timestamp Report Message, corresponding to PrevTRMSeqNum. The LSBit of the Timestamp corresponds to a time of 0.030517578125μsec = one clock tick at 32.768MHz. The Timestamp will rollover every 131 seconds = 2.2 minutes.
NumSlots	1 octet	Number of Slot Timestamps specified in the payload of this control message. NumSlots may be zero. Each Slot Timestamp is accompanied by a MACAddr, and Channel_ID field. Including the Slot Timestamp, each Slot Timestamp is 12 bytes long.
PAD_0	3 octets	Padding to align to a 32-bit boundary. Always present, even when NumSlots has the value of 0.
MACAddr	6 octets	MAC Address associated with the immediately following Channel_ID and STimestamp.
Channel_ID	2 octets	Identifier for a channel associated with the immediately preceding MACAddr.
STimestamp	4 octets	Slot Timestamp corresponding to the immediately preceding Channel_ID. This is the time at which the TRM sender wishes to receive a future constant bit rate service flow packet in order to minimize overall latency of delivery to a synchronous network. The time value corresponds to the time at the timing master. Additional packets for the identified service flow are expected to arrive at periodic intervals measured from this time. The LSBit of the STimestamp corresponds to a time of 0.030517578125μsec = one clock tick at 32.768MHz.
MACAddr	6 octets	MAC Address associated with the immediately following Channel-ID and STimestamp.
Channel_ID	2 octets	Identifier for a channel associated with the immediately following Channel_ID and STimestamp.

FIG. 85(2)

Field	Length	Meaning
STimestamp	4 octets	Slot Timestamp corresponding to the immediately preceding Channel_ID. This is the time at which the TRM sender wishes to receive a future constant bit rate service flow packet in order to minimize overall latency of delivery to a synchronous network. Additional packets for the identified service flow are expected to arrive at periodic intervals measured from this time. The LSBit of the STimestamp corresponds to a time of 0.030517578125μsec = one clock tick at 32.768 MHz.
...		[additional instances of MACAddr, Channel_ID and Gtimestamp fields, until the number of Gtimestamp fields equals NumGrants]
Next Ethertype	2 octets	= 0
Pad	max (0,44-SSLength octets	Any value octet
FCS	4 octets	

FIG. 85(3)

Field	Length	Meaning
DA	6 octets	Destination Address (FF.FF.FF.FF.FF.FF)
SA	6 octets	Source Address
Ethertype	2 octets	0x886c (HPNA Link Control Frame)
SSType	1 octet	= 6
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field and ending with the second (last) octet of the Next Ethertype field. Minimum is 4.
SSVersion	1 octet	= 0
TRM_type	1 octet	Value of x80 means that this is a TQM.
Next Ethertype	2 octets	= 0
Pad	MIN(0,40-SSLength) octets	Any value octet
FCS	4 octets	

FIG. 86

Field	Length	Meaning
DA	6 octets	Destination Address (FF.FF.FF.FF.FF.FF)
SA	6 octets	Source Address
Ethertype	2 octets	0x886c (HPNA Link Control Frame)
SSType	1 octet	= 6
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field and ending with the second (last) octet of the Next Ethertype field. Minimum is 4.
SSVersion	1 octet	= 0
TRM_type	1 octet	Value of x81 means that this is a TSM.
Next Ethertype	2 octets	= 0
Pad	MIN(0,40-SSLength) octets	Any value octet
FCS	4 octets	

FIG. 87

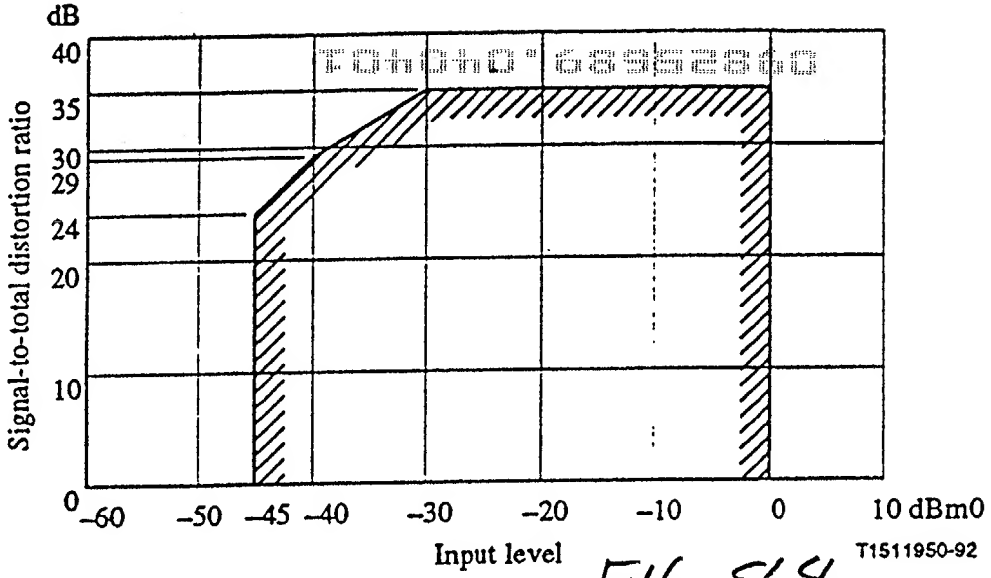


FIG. 88

Input Level	Uniform Quantizer + Compander SNR	The required SNR for the ADC/DAC
0 dBm	38.43 dB	60 dB
-30 dBm	35.50 dB	54 dB
- 40 dBm	30.09 dB	44 dB

FIG. 89a

Input Level	G.712 SNR Spec	The total SNR with Uniform Quantizer + Compander + jitter Clock
0 dBm	35 dB	38.32 dB (60 dB ADC/DAC SNR is used)
-30 dBm	35 dB	35.42 dB (54 dB ADC/DAC SNR is used)
- 40 dBm	29 dB	30.05 dB (44 dB) ADC/DAC SNR is used)

FIG. 89b

Input Level	G.712 SNR Spec	The total SNR with Uniform Quantizer + Compander + jitter Clock
0 dBm	35 dB	38.38 dB (60 dB ADC/DAC SNR is used)
-30 dBm	35 dB	35.26 dB (54 dB ADC/DAC SNR is used)
- 40 dBm	29 dB	30.03 dB (44 dB) ADC/DAC SNR is used)

FIG 89c

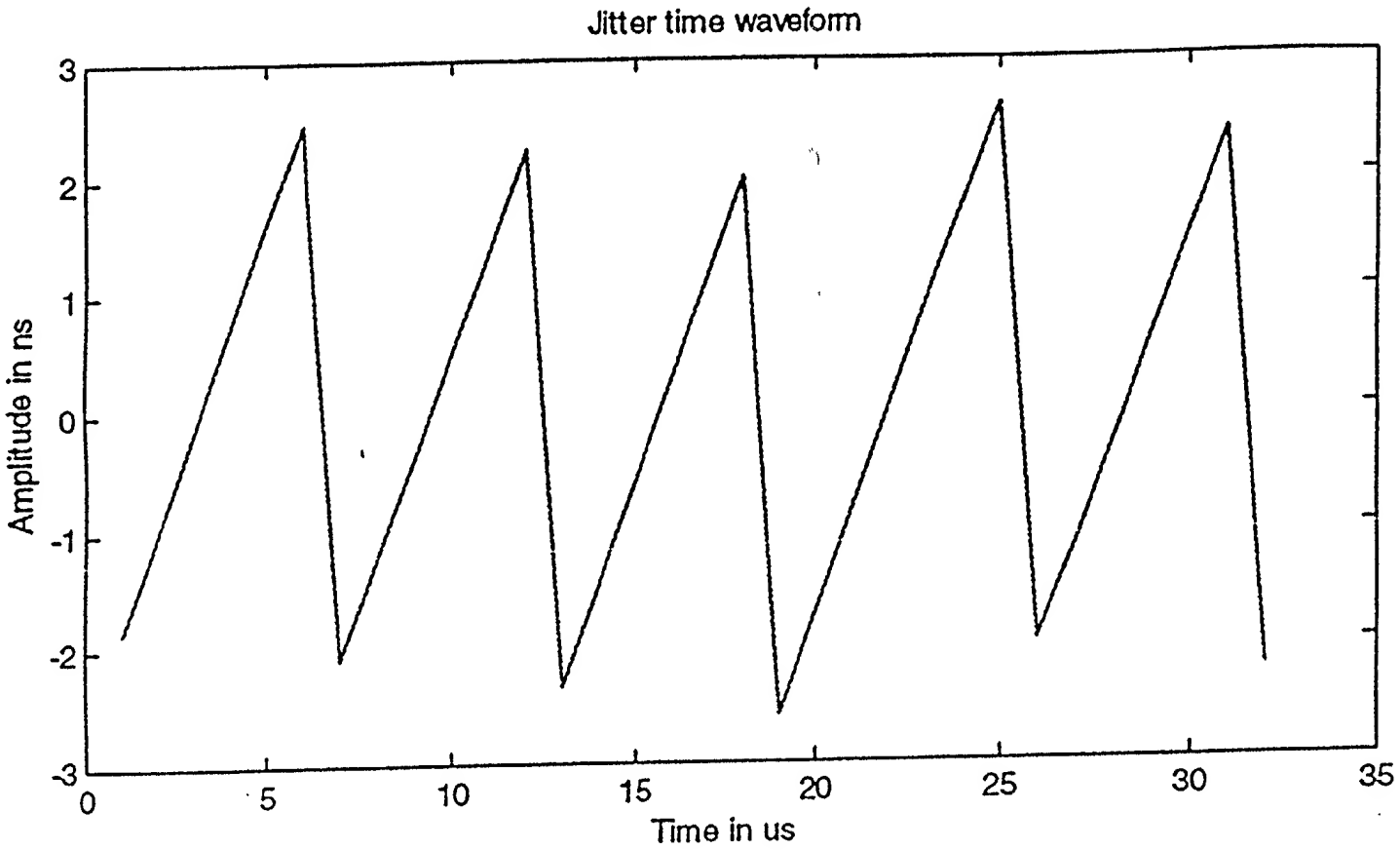

Jitter time waveform
Amplitude in ns
Time in us
3
2
1
0
-1
-2
-3
0
5
10
15
20
25
30
35

FIG. 9D

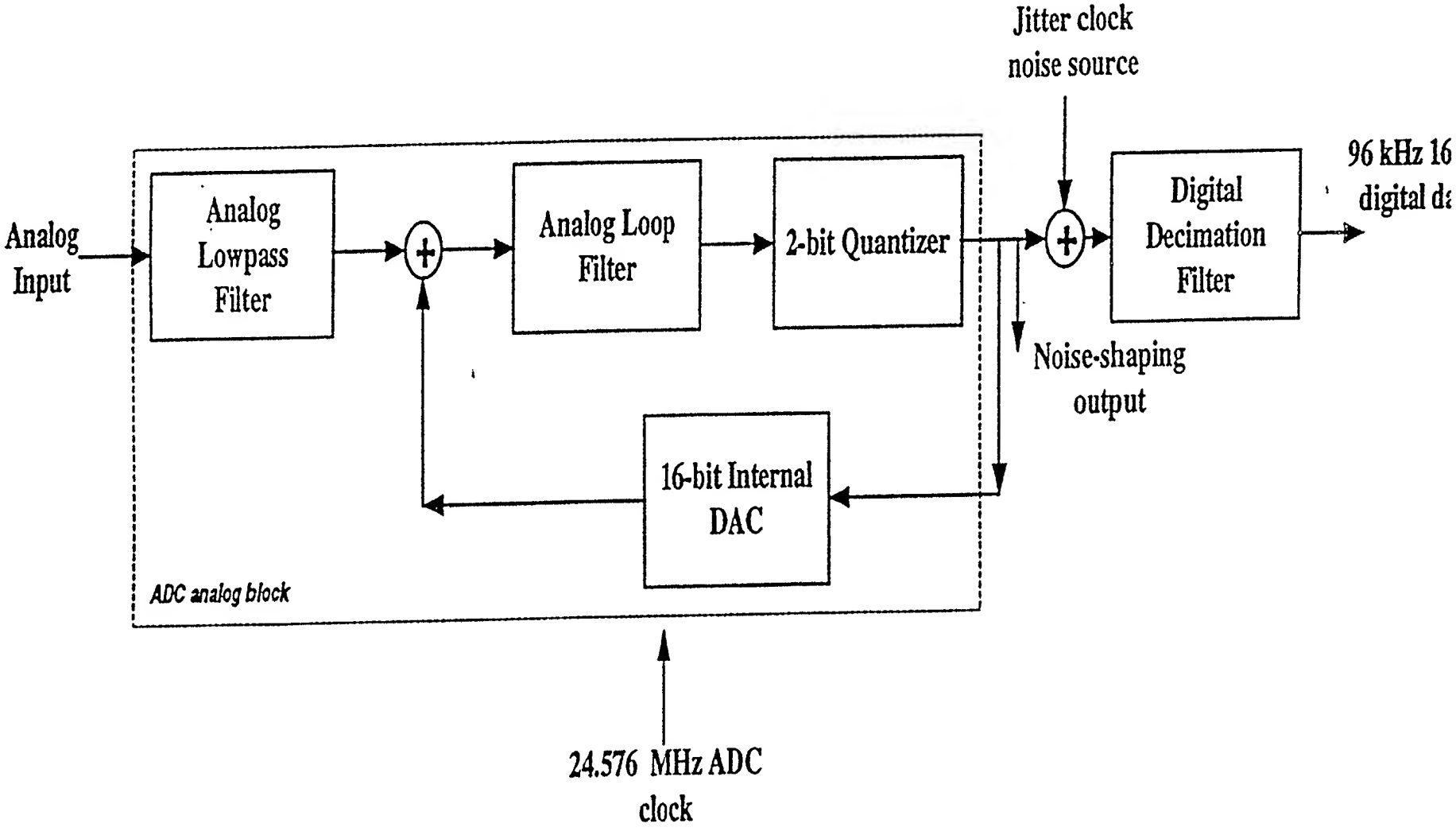

Jitter clock
noise source
Analog
Input
Analog
Lowpass
Filter
Analog Loop
Filter
2-bit Quantizer
Digital
Decimation
Filter
96 kHz 16
digital da
Noise-shaping
output
16-bit Internal
DAC
ADC analog block
24.576 MHz ADC
clock

FIG. 91

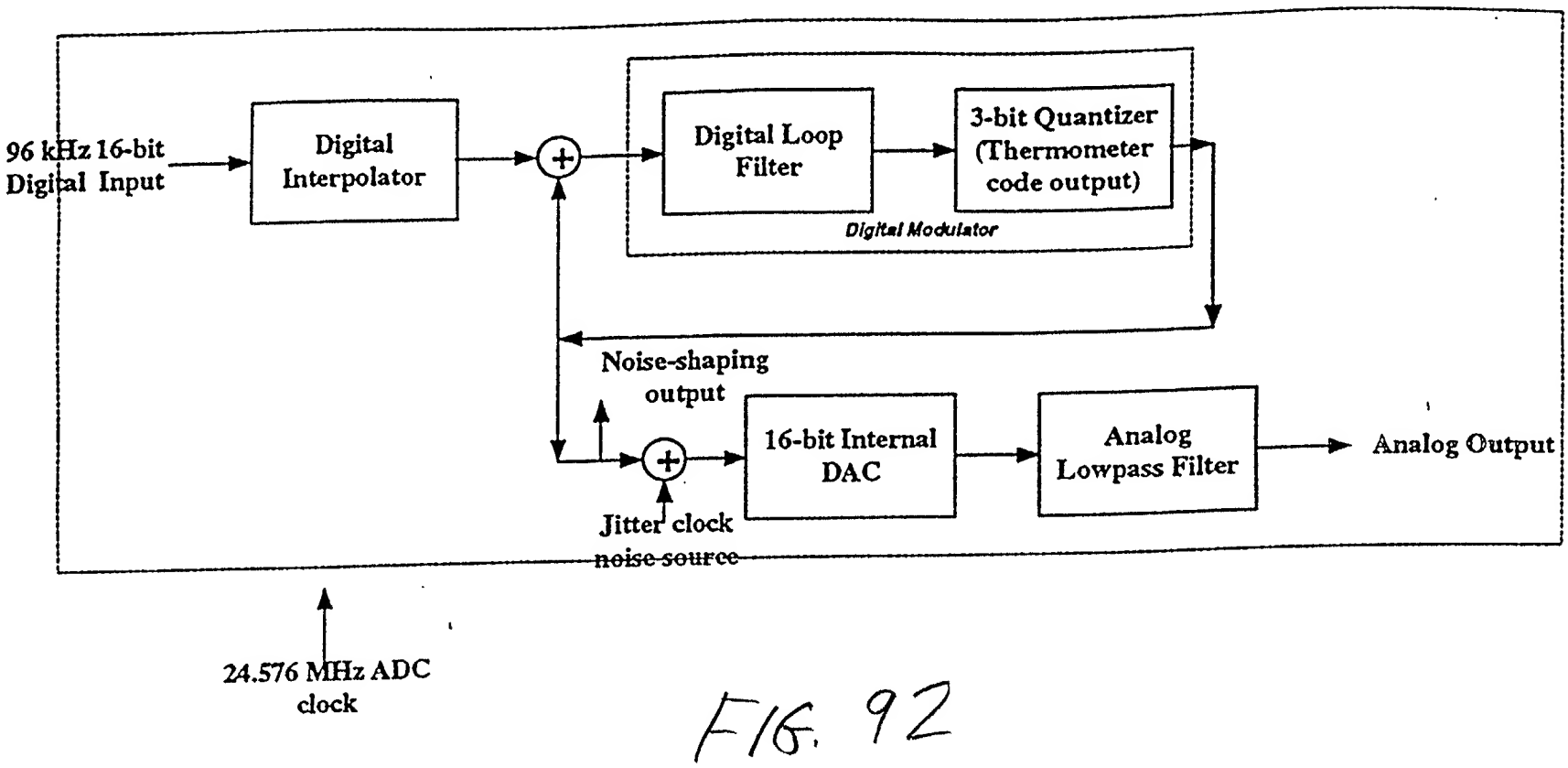

96 kHz 16-bit
Digital Input
Digital
Interpolator
Digital Loop
Filter
3-bit Quantizer
(Thermometer
code output)
Digital Modulator
Noise-shaping
output
16-bit Internal
DAC
Analog
Lowpass Filter
Analog Output
Jitter clock
noise source
24.576 MHz ADC
clock

FIG. 92

Octet	Field	Length	Description
Flags 0	TxPriority7	1	Station is (was) transmitting frames with LL priority 7. (always set)
	TxPriority6	1	Station is (was) transmitting frames with LL priority 6.
	TxPriority5	1	Station is (was) transmitting frames with LL priority 5.
	TXPriority4	1	Station is (was) transmitting frames with LL priority 4.
	TxPriority3	1	Station is (was) transmitting frames with LL priority 3.
	TxPriority2	1	Station is (was) transmitting frames with LL priority 2.
	TxPriority1	1	Station is (was) transmitting frames with LL priority 1.
	TxPriority0	1	Station is (was) transmitting frames with LL priority 0. (always set)
Flags 1	Reserved	5	Shall be sent as 0 and ignored by 2.0 stations when received.
	CSS_Master_Capability	1	This station is capable of operating as a CSS Master node.
	No_V1M2_Frames	1	This station does not support the reception or transmission of compatibility frames (V1M2 frames).
	Supports 4Mbaud	1	This station supports 4 megabaud payload encodings.
Flags 2	Reserved	8	Shall be sent as 0 and ignored by 2.0 stations when received.
Flags 3	ConfigV2	1	Force use of 10M8 mode, defers to Config1 and ConfigV1Ms.
	ConfigV1M2	1	Force use of HPNA V1M2 mixed mode, defers to ConfigV1.

FIG. 93(1)

Octet	Field	Length	Description
	ConfigV1	1	Force use of HPNA 1.x mode, highest precedence of config flags.
	Reserved	2	Shall be sent as 0 and ignored by 2.0 stations when received.
	Highest Version	3	This station's highest supported HPNA version: 0x000 -- Reserved 0x001 -- HPNA 1.0 0x010 -- HPNA 2.0 0x001-0x111 Reserved

F16. 93(2)

Field	Length	Meaning
CSEType	1 octet	X00 = signifies a CSS Extension type
CSELength	1 octet	X08 = Number of additional octets in this CSEType. CSELength is always x08 for CSEType = x00 = CSS
CSS_MAC	6 octets	MAC address of client station
CSS_SEQ	2 octets	CSS sequence, 8 two-bit values concatenated: 0-2 indicate a specific signaling slot, while 3 indicates the use of a randomly selected value chosen by the client at the time of the collision. X0000 - xBFFF = assigned CSS_SEQ value for the node possessing the MAC address specified in CSS_MAC XC000 - xFEFF = reserved XFF00 = indication by the client node specified by CSS_MAC that it is no longer an active sender of link layer priority 6 frames (equivalent to a "0 active channels" indication) XFF01 - xFFFE = request by the client node specified by CSS_MAC for a CSS Sequence from the master node. The 8 Least significant bits indicate the number of active channels which are sending link layer. priority 6 frames for this client. XFFFF - reserved

FIG. 94

2-bit CSS register value (binary)	Signal slot integer (decimal)
00	0
01	1
10	2
11	Random in range [0,2]

FIG. 95

Bit Number	Value
7:0	**Station Type:** 0 – HomePNA 1.x station 1 – 10M8 station in V1M2 Mode 2 – 10M8 station in V1M2 Mode, that has detected a recent 1M8 transmission with PCOM Station Type = 0 Other values reserved
31:8	Reserved, must be 0 on transmission

FIG. 96

Precedence	Variable
1	ConfigV1
2	ConfigV1M2
3	ConfigV2
4	V1_DETECTED
4	V1_SIGNALED

FIG. 97